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CONTROL DATA CORPORATION

CORE-RESIDENT REAL-TIME MAINTENANCE SYSTEM USERS GUIDE

CDC® COMPUTER SYSTEM:
1700

PRELIMINARY

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APPENDIX A

MONITOR DESCRIPTION

GENERAL DESCRIPTION

The CONTROL DATA® 1700 Core Resident Real Time Maintenance System (CRRTMS) is a self contained diagnostic system for the 1700 computer family and its related peripherals. CRRTMS is made up of three parts: Monitor, Diagnostic Supervisor and an expandable set of test routines belonging to a class of diagnostics which use, where possible, the standard 1700 Mass Storage Operating System (MSOS) Input/Output drivers for all communication with the device under test. The Core Resident Monitor (CRM) is an MSOS 3.0 based monitor with certain modifications to allow the running of MSOS 4.X or MSOS 5.0 drivers. A number of modifications have been made to allow the dynamic allocation of interrupt lines, priorities and logical units, loadable test routines with their associated MSOS drivers and physical device tables; and an expandable monitor that will not affect entry points of test routines.

MINIMUM CONFIGURATIONS

The minimum configurations required for loading and executing CRRTMS are as follows:

1704, 1705 CPU with 8K of core memory and A/D/DSA channels.
1711 or 1713 Teletype and one of the following load devices:

1721 Paper Tape Reader
1729-2 Card Reader
1728/430 Card Reader/Punch
1731/601 Mag Tape Subsystem
1732/608/609 Mag Tape Subsystem
1738/853/854 Disk Subsystem

1714 (32K mode only) CPU with 24K of core memory and A/D-DSA channels
1711 or 1713 Teletype and one of the following load devices:

1729-2 Card Reader
1728/430 Card Reader/Punch
1731/601 Mag Tape Subsystem
1732/608/609 Mag Tape Subsystem
1738/853/854 Disk Subsystem

1774, 1773, 1775, 1772 CPU with 8K of core memory and A/Q-DSA channels
1711 or 1713 Teletype and one of the following load devices:

1777 Paper Tape Station
1729-2 Card Reader
1728/430 Card Reader/Punch
1731/601 Mag Tape Subsystem
1732/608/609 Mag Tape Subsystem
1738/853/854 Disk Subsystem

1784-X, 1782-X (32K mode only) CPU with 8K of MOS memory and TTL A/Q-DSA channel
1711, 1713 Teletypes or 713-10 CRT and one of the following load devices:

1777 Paper Tape Station*
1729-2 Card Reader*
1728/430 Card Reader/Punch*
1731/601 Mag Tape Subsystem*
1732/608/609 Mag Tape Subsystem*
1732-2/856-2/856-4/856-12/856-14 Cartridge Disk Subsystem

18-10M, 18-20 or 18-30TS Processors (32K mode only) and 1882-16 MOS Main Memory
1811-1 or 1811-2 Console CRT and one of the following Load devices:

1828-1/1829-30/1829-60 Card Reader
1833-5/1865-1/1865-2 Flexible Disk Subsystem

Recommended, but not required:

1750, 1572 Sample Rate Generator
or
1750, 1573 Line Sync Clock
or
1750-1, 1572-1 Sample Timing Unit

*Requires 1785-3 1700 A/Q Channel Adapter

GENERAL DESCRIPTION

CRRTMS is available in several mediums: punched cards, paper tape, seven or nine track mag tape, disks and flexible diskettes. Loading the monitor diagnostic supervisor and the test routines requires two steps. The monitor and diagnostic supervisor are loaded in the first step. Once loaded, the initialization of the monitor is done in conversational mode via the console TTY or CRT display. This initialization is described in this section. The second load operation is performed by the monitor at the command of the user to load desired test routines. This load operation is described in the next section.

LOADING MONITOR

For punched cards, paper tape and mag tape, loading the monitor and diagnostic supervisor requires using a hand entered Bootstrap. Figures 2.1 thru 2.5 list these bootstraps for the supported load devices. In all cases, the bootstrap should be loaded in the highest memory location. If loading is successful, the bootstraps will start execution at memory location 0001.

Enter the required bootstrap in the following manner:

a. Master Clear

b. Set PROGRAM PROTECT switch to the center position.

c. If 1714 or 1784, set MODE switch in 32K mode

d. Press P register select button.

e. Set P register to $XFB0 {X = number of highest memory bank}.

f. Set ENTER/SWEEP switch to ENTER.

g. If 1784, set INSTRUCTION/CYCLE switch to CYCLE.

h. Press X register select button.

i. Clear X register with clear button.

j. Enter word of bootstrap in X {see Figures 2.1 through 2.5

k. Push RUN/STEP switch to STEP; if a 1784, push GO button.

l. Repeat steps i, j and k until bootstrap has been entered.

m. Return ENTER/SWEEP switch to center position.

n. If a 1784, return INSTRUCTION/CYCLE switch to center position.

o Master Clear

p. Make input device READY.

q. Press P register select button.

r. Set P register to $XFB0 (first word address of Bootstrap).

s. Push RUN/STEP switch to RUN; if a 1784, push GO button.

If the loading of the bootstrap is successful, execution of the monitor will automatically result. If it does not, an error has occurred. Check that the correct hardware address was inserted in the bootstrap during entry. If the bootstrap is stopped on a $18FF, it means the bootstrap detected a sum error during loading.

If the load device is a 1738/85X Disk or a 1733-2/856-X cartridge disk, no bootstrap is required because of the controller autoload feature. Use the following procedure:

a. Master Clear

b. Set PROGRAM PROTECT switch to the center position.

c. If a 1714 or 1784, set MODE switch in 32K mode.

d. Make sure the disk drive is ready.

e. Set SELECTIVE STOP switch if the disk controller wquipment number is not 3 (i.e. WES code = $0181) or unit number of disk drive is not to be zero.

f. Press AUTOLOAD button.

g. Push RUN/STEP switch to RUN; if a 1784, push GO button.

h. If the SELECTIVE STOP switch is not set, execution of monitor will start. If SELECTIVE STOP switch is set, the CPU will stop with the WES code in 'Q' register and the unit selection function in 'A' register. Change contents of registers as required, set SELECTIVE STOP switch to off position and press GO button.

If the load device is a 1833-5/1865-X Flexible Disk, no bootstrap is required because of the controller deadstart feature. Use the following procedure:

a. Master Clear

b. Insert Diskette in drive unit ZERO.

c. Insure that all other deadstart devices are in a not ready state (i.e. Card reader and/or Cassettes).

d. Press Deadstart.

Deadstart will load a bootstrap which in turn will load the monitor and start execution. If after several repeats the monitor does not start into execution, the WES code in the bootstrap loaded may be incorrect. It is prestored as $0385. If this is not the correct WES code, enter this on the CRT:

a. Excape (ESC)

b. type HG

c. type J04G

d. type L0XX5G where XX is proper WES code

e. type J03G

f. type K1F02G

g. type I

The monitor should now be loaded and start execution.

MONITOR INITIALIZATION

Once execution of the monitor has started, all communication is done via the console TTY or CRT. This communication is a conversational input/output. The TTY or CRT are referred to as the Standard Input Comment Medium (SICM) and the Standard Output Comment Medium (SOCM) when discussing the operator interaction via the TTY or CRT. The operator must take care to enter the requested information as described below carefully as each field cannot always be absolutely checked for errors.

The intialization routine allows the user to input the required system configuration information: computer type; timer type (if any), interrupt line number and WES code; loader interrupt line and WES code. This information can only be input during initialization as this routine is over-written after initialization is complete.

When execution of the monitor begins, an informational title message is output on the SOCM as follows:

CRRTMS 2.0 LEVEL XXX (MM/DD/YY)

where XXX is the Program Summary Level number of the last change to the system

MM are the month, day and
DD year CRRTMS system was
YY initialized

These two items should be referenced any time a trouble report is issued.

Following the output of the title, a request message is output on the SOCM as follows:

CPU MODEL NUMBER

The initialization routine then enables the SICM for operator keyboard input of 4 or 6 characters in the following format:

(Field) (CR)

Where Field indicates the entry of one of the following model numbers:

1704, 1714, 1774, 1784-1, 18-17A, 1784-2, 18-17B, 18-10, 18-10M, 18-20, 18-30, 18-30TS.

(CR) indicates the input of a carriage return.

If the characters input do not agree with one of the model numbers specified, the request message is repeated and input is again enabled.

Following correct input of the CPU model number, another request message is output on the SOCM as follows:

```
SYSTEM TIMER
TYPE, LINE FREQ
```

The SICM keyboard is then enabled for operator input of two control parameters in the following format:

{Field 1}, {Field 2} (CR)

Where Field 1 is defined as follows:

0 = no timer
1 = 1573 Line Sync Clock
2 = 1572 Sample Rate Generator
3 = 1572-1 Sample Timing Unit
4 = CYBER 18 CPU Clock

Field 2 decimal value of the power line frequency in HZ {cps}

(CR) Carriage Return

If zero is entered for timer type, the next message is deleted and a simulated timer is used.

Following a non-zero entry (1, 2 or 3) for the timer type, a request message is output on the

{Timer Name} INT LINE, WES CODE

Where Timer Name is one of the following:

1573 LSC
1572 SRG
1572-1 STU

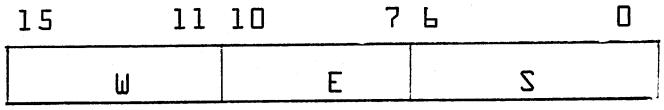
The SICM keyboard is then enabled for operator input of two control parameters in the following format:

{Field 1}, {Field 2} (CR)

where Field 1 — decimal interrupt line number in the range 2 to 15. If not, the following message is output and the request is repeated.

INTERRUPT ENTRY ERROR

Field 2 — the hexidecimal number that is loaded into the 'Q' register to address the timer requested.



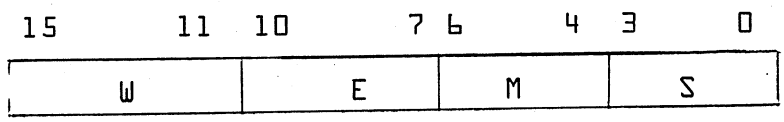
where W = converter code which must always be zero.

E = equipment number of the 1750 to which the timer is connected.

S = station address of the timer

1573 - S=0
1572 - S=2
} normally

If a 1572-1 was requested, the message is changed to WEMS CODE and 'Q' is defined as:



where W = same
E = same
M = module holding the timer
S = slot number of the timer within the module.

(CR) Carriage Return

If timer type 4 was entered, the following message is output on the SOCM instead of the above sequence:

```
CYBER 18 CPU CLOCK
MACRO/MICRO INT LINE
```

The SICM keyboard is then enabled for operator input of one control parameter as follows:

{Field} (CR)

where Field = the decimal interrupt line number in the range 2 to 12. If not, the following message is output and the request is repeated

INTERRUPT ENTRY ERROR

Only one field is requested as the WES code of the CPU Clock is fixed as $00F0.

Next, {continue here is no timer} a request message is output on the SOCM as follows:

```
{Loader Name} LOADER
INT LINE, WES CODE
```

where: Loader Name is one of the following:

CARD READER for the 1726/405, 1728/430, 1729-2, 1729-3 or 1829-30/60 readers.

MAG TAPE for the 1732-1/608/609 or 1732-3/616-72/616-92/616-95 mag tape subsystems.

PAPER TAPE for the 1721, 1722, 1777 or 1720-1 paper tape readers.

1738/85X DISK for the 1738/853/854 disk drive.

1733-2 CARTRIDGE DISK for the 1733-2/856-X cartridge disk drive.

1833-5 FLEXIBLE DISK for the 1833-5/1865-X flexible disk drive.

Each monitor has only one loader, that loader is for the medium which was bootstrapped or autoloaded.

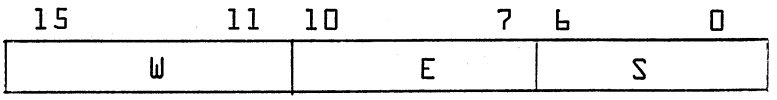
The SICM keyboard is then enabled for operator input of two control parameters in the following format:

{Field 1}, {Field 2} (CR)

where Field 1 decimal interrupt line number in the range 1 to 15. If not, the following message is output and the request is repeated.

INTERRUPT ENTRY ERROR

Field 2 is the hexadecimal number that is loaded into the 'Q' register to address the loader device



Where W = the converter code which must be zero if the loader device is not connected via a 1706 BDC or the value for direct data transfer if the loader device is connected via a 1706 BDC (see 1700 Codes Book).

E = equipment number of the loader device

S = the station address of the loader device for Level 1 status and functions

(CR) Carriage Return

If the loader device is a Card Reader, then the following request message is output on SOCM before initialization is complete.

IS C.R. a 1726/405?

The operator must enter one of the following:

NO or 0 (zero) if the card reader is a 1728/430, 1729-2 or 1729-3

YES or 1 (Non-zero) if the card reader is a 1726/405

followed by a (CR)

When all the above input requested is input, the initialization routine is complete. This routine cannot be recalled because it is overlayed when the first test routine is loaded.

If the monitor was loaded from the 1833-5/1865-X, Flexible Disk, the system is preconfigured and starts up as follows:

```
CRRTMS 2.0 LEVEL XXX (MM/DD/YY)
CYBER 18 PROCESSOR
CPU CLOCK
INT LINE = 8, WES CODE = $00F0
1833-5 FLEXIBLE DISK LOADER
INT LINE = 7, WES CODE = $0380
INT LINE = 7, WES CODE = $0380
DO YOU WISH TO CHANGE CONFIGURATION INFO?
```

The operator must enter one of the following:

NO or 0 (zero)	if the configuration information is correct. If entered, the program goes directly to start up routine.
YES or 1 (non-zero)	If the configuration information is to be changed. If entered, program goes to system timer information request.

If the monitor is started up in the 65K mode, the following message will be output and the system will hang:

```
CRRTMS 2.0 - CPU IN 65K MODE
MASTER CLEAR, PUT IN 32K MODE AND RESTART
```

START UP ROUTINE

When the initialization routine is completed or when the CPU is master cleared and subsequently restarted, the start up routine is entered. This routine uses the information input in the initialization routine to start up the system timer and prepare for test routine loading.

First, the timer type is checked and if no timer was specified, the following message is output on the SOCM:

NO TIMER

All system timing is accomplished by a simulated timer routine in the idle loop. Control is then transferred to ready message.

If the timer type was not zero, then an attempt is made to allocate and initialize the timer interrupt line and interrupt trap region. If this initialization is not completed without error, the message NO TIMER is output and the conditions above apply.

If the timer interrupt setup occurs without error, the timer interrupt is enabled via a function output to the hardware address specified during the initialization routine.

If a reject occurs during the output of the enable function, the following message is output on the SOCM:

TIMER REJ

The interrupt line setup is released and the same conditions as NO TIMER apply.

If no timer reject occurs, the timer should now be enabled and interrupt the system at a rate of 50 or 60Hz. These interrupts will override the simulated timer.

In all cases, the following message is output to notify the user that the system is ready for operator commands.

MANUAL INTERRUPT TO START

Following the output of the message, the manual interrupt lockout flag is cleared and the system waits in the IDLE loop for operator action.

Once the initialization routine is complete, the system may be restarted at anytime by Master Clearing the CPU and

setting RUN. All tests currently loaded in memory will remain linked to the monitor, but all flags will be cleared. If restart is executed while a load operation is in progress, the skip switch should be set to restore the memory allocation thread. This will destroy all links to tests previously loaded.

Be careful not to restart monitor in 64K mode as this could destroy integrity of the monitor itself. If the CPU is an 18-10M, 18-20 or 18-30TS, then the Function Control Register (FCR) must be set up before starting execution as follows:

Master Clear

Type ESC

Type K31002800G

Type K0000G

Type I@

Monitor will be restarted.

EXAMPLE 1

OPERATOR EXAMPLES

CRRTMS 2.0 LEVEL 120 {07/01/77}	Monitor Output
CPU MODEL NO.	Monitor Output
1704 (CR)	Operator Input
SYSTEM TIMER	Monitor Output
TYPE, LINE FREQ	Monitor Output
1,60 (CR)	Operator Input
1573 LSC INT LINE, WES CODE	Monitor Output
8,400 (CR)	Operator Input
CARD READER LOADER	Monitor Output
INT LINE, WES CODE	Monitor Output
11,5A1 (CR)	Operator Input
IS C.F. A 1726/405?	Monitor Output
NO (CR)	Operator Input
MANUAL INTERRUPT TO START	Monitor Output

EXAMPLE 2

CRRTMS 2.0 LEVEL 120 {07/01/77}	Monitor Output
CPU MODEL NO.	Monitor Output
1784 (CR)	Operator Input
CPU MODEL NO.	Monitor Output
1784-1 (CR)	Operator Input
SYSTEM TIMER	Monitor Output
TYPE, LINE FREQ	Monitor Output
0 (CR)	Operator Input
CARD READER LOADER	Monitor Output
INT LINE, WES CODE	Monitor Output
17, 5A1 (CR)	Operator Input
INT LINE ENTRY ERROR	Monitor Output
CARD READER LOADER	Monitor Output
INT LINE, WES CODE	Monitor Output
11,5A1 (CR)	Operator Input
IS C.R. A 1726/405?	Monitor Output
NO (CR)	Operator Input
NO TIMER	Monitor Output
MANUAL INTERRUPT TO START	Monitor Output

START UP ROUTINE

EXAMPLE 3

```
CRRTMS 2.0 LEVEL 120 (07/01/77)          Monitor Output
CPU MODEL NO.                            Monitor Output
1784-1 (CR)                              Operator Input
SYSTEM TIMER                             Monitor Output
TYPE, LINE FREQ                          Monitor Output
3,60   (CR)                              Operator Input
1572-1 STU INT LINE, WEMS CODE           Monitor Output
8,048F (CR)                              Operator Input
MAG TAPE LOADER                          Monitor Output
INT LINE, WES CODE                       Monitor Output
15,1381 (CR)                             Operator Input
TIMER REJ                                Monitor Output
MANUAL INTERRUPT TO START                Monitor Output
```

```
XFB0        0AFE                ENA     -1
  1         6824                STA*    CORLOC
  2         E000      FEED      LDQ     =N$WESD
  3         WESD                        (i.e. 05A1)
  4         C000                LDA     =N$0081
  5         0081
  6         03FE                OUT     -1
  7         0AD7                ENA     -40
  8         681E                STA*    COLCNT
  9         0DFE                INQ     -1
  A         02FE      NXTCOL    INP     -1
  B         A81D                AND*    MASK
  C         0FC8                ALS     8
  D         6C18                STA*    (CORLOC)
  E         02FE                INP     -1
  F         A819                AND*    MASK
XFC0        BC15                EOR*    (CORLOC)
  1         6C14                STA*    (CLORLOC)
  2         0829                AAM     M       .
  3         C812                LDA*    CORLOC
  4         0123                SAP     NOTIST-*-1
  5         CC10                LDA*    (CORLOC)
  6         6811                STA*    WRDCNT
  7         1804                JMP*    FIRST
  8         C80F      NOTIST    LDA*    WRDCNT
  9         0107                SAZ     DONE-*-1
  A         D80D                RAO*    WRDCNT
  B         D80A      FIRST     RAO*    CORLOC
  C         D80A                RAO*    COLCNT
  D         C809                LDA*    COLCNT
  E         0121                SAP     NXTCRD-*-1
  F         18EA                JMP*    NXTCOL
XED0        18E1      NXTCRD    JMP*    FEED
  1         080C      DONE      TRM     A
  2         0101                SAZ     GOSTRT-*-1
  3         18FF                JUMP*   *-0
  4         1401      GOSTRT    JMP-    (1)
  5         0000      CORLOC    NUM     0
  6         0000      COLCNT    NUM     0
XFD7        0000      WRDCNT    NUM     0
XFD8        00FF      MASK      NUM     $FF
```

Figure 2.1 1728/430,1729-2, 1729-3
CARD READER BOOTSTRAP

```
XFB0      0AFE                ENA     -1
   1      6822                STA*    CORLOC
   2      E000                LDQ     =N$WESD
   3      WESD                        (i.e. 0581)
   4      C000                LDA     =N$0401
   5      0401
   6      03FE                OUT     -1
   7      0DFE                INQ     -1
   8      02FE    NXTCOL      INP     -1
   9      A81C                AND*    MASK
   A      0FC8                ALS     8
   B      6C18                STA*    (CORLOC)
   C      02FE                INP     -1
   D      A818                AND*    MASK
   E      BC15                EOR*    (CORLOC)
   F      6C14                STA*    (CORLOC)
XFC0      0829                AAM     M
   1      C812                LDA*    CORLOC
   2      0123                SAP     NOTIST-*-1
   3      CC10                LDA*    (CORLOC)
   4      6810                STA*    WRDCNT
   5      1804                JMP*    FIRST
   6      C80E    NOTIST      LDA*    WRDCNT
   7      0103                SAZ     DONE-*-1
   8      D80C                RAO*    SRDCNT
   9      D80A    FIRST       RAO*    CORLOC
   A      18ED                JMP*    NXTCOL
   B      080C    DONE        TRM     A
   C      0101                SAZ     GOSTRT-*-1
   D      18FF                JMP*    *-0
   E      0D01    GOSTRT      INQ     +1
   F      C000                LDA     =N$1000
XFD0      1000
   1      03FE                OUT     -1
   2      1401                JMP-    (1)
   3      0000    CORLOC      NUM     0
   4      0000    WRDCNT      NUM     0
   5      00FF    MASK        NUM     $FF
```

Figure 2.2 1726/405
CARD READER BOOTSTRAP

```
XFB0      6820                STA*    CORLOC
  1       E000                LDQ     =N$WESD
  2       WESD                        {i.e. 0382 or 1382}
  3       C000                LDA     =N$0414
  4       0414
  5       03FE                OUT     -1
  6       0DFE                INQ     -1
  7       09EC                INA     -$13
  8       03FE                OUT     -1
  9       0F42                ARS     2
  A       03FE                OUT     -1
  B       0DFE    NXTWRD      INQ     -1
  C       0A00                ENA     0
  D       020C                INP     CKEOP-*-1
  E       0FCA                ALS     10
XFBF      0821                TRA     M
XFC0      0A00                ENA     0
  1       02FE                INP     -1
  2       0FC4                ALS     4
  3       0869                EAM     M
  4       0A00                ENA     0
  5       02FE                INP     -1
  6       0F42                ARS     2
  7       086C                EAM     A
  8       6C08                STA*    {CORLOC}
  9       D807                RAO*    CORLOC
  A       0D01    CKEOP       INQ     +1
  B       02FE                INP     -1
  C       0FCB                ALS     11
  D       0131                SAM     EOP-*-1
  E       18EC                JMP*    NXTWRD
XFCF      1401    EOP         JMP-    {1}
XFD0      0000    CORLOC      NUM     0

          LOAD MAG TAPE ON UNIT 0
```

Figure 2.3 1731/601, 1732-1/608, 1732-3/616-72 7-TRACK MAG TAPE BOOTSTRAP

```
XFB0    6815                STA*    CORLOC
  1     E000                LDQ     =N$WESD
  2     WESD                        {i.e. 1382 or D382}
  3     C000                LDA     =N$0444
  4     0444
  5     03FE                OUT     -1
  6     0DFE                INQ     -1
  7     09BC                INA     -$43
  8     03FE                OUT     -1
  9     0F42                ARS     2
  A     03FE                OUT     -1
  B     0DFE    NXTWRD      INQ     -1
  C     0202                INP     CKEOP-*-1
  D     6C08                STA*    {CORLOC}
  E     D807                RAO*    CORLOC
XFBF    0D01    CKEOP       ENQ     +1
XFC0    02FE                INP     -1
  1     0FCB                ALS     11
  2     0131                SAM     EOP-*-1
  3     18F7                JMP*    NXTWRD
  4     1401    EOP         JMP-    {1}
XFC5    0000    CORLOC      NUM     0

        LOAD MAG TAPE ON UNIT 0
```

Figure 2.4 1732/609, 1733-2/616-92/95 {9 TRACK} MAG TAPE BOOTSTRAP

```
XFB0    0AFE                ENA     -1
  1     681C                STA*    CORL0C
  2     E000                LDQ     =N$00A1
  3     00A1
  4     0A20                ENA     $20
  5     03FE                OUT     -1
  6     0DFE                INQ     -1
  7     02FE                INP     -1
  8     0112    LDR         SAN     DATA-*-1
  9     18FD                JMP*    LDR
  A     02FE    NXTDAT      INP     -1
  B     0FC8    DATA        ALS     8
  C     02FE                INP     -1
  D     6C10                STA*    (CORL0C)
  E     0829                AAM     M
XFBF    C80E                LDA*    CORL0C
XFC0    0123                SAP     NOTIST-*-1
  1     CC0C                LDA*    (CORL0C)
  2     680C                STA*    WRDCNT
  3     1804                JMP*    FIRST
  4     C80A    NOT1ST      LDA*    WRDCNT
  5     0103                SAZ     DONE-*-1
  6     D808                RA0*    WRDCNT
  7     D806    FIRST       RA0*    CORL0C
  8     18F1                JMP*    NXTDAT
  9     080C    DONE        TRM     A
  A     0101                SAZ     GOSTRT-*-1
  B     18FF                JMP*    *-0
  C     1401    GOSTRT      JMP-    (1)
  D     0000    CORL0C      NUM     0
XFCE    0000    WRDCNT      NUM     0
```

Figure 2.5 1720, 1721, 1777
PAPER TAPE BOOTSTRAP

GENERAL DESCRIPTION

The loading and controlling of test routines is done via the Diagnostic Supervisor using descriptive control words. These control words are input via the console TTY or CRT. Each of the control words is checked for its validity and error messages are output when control words are improperly input.

CONTROL WORD INPUT

When the user causes a manual interrupt, MI, and the manual interrupt lockout flag is not set, the Diagnostic Supervisor is scheduled. On entry to the Diagnostic Supervisor, the manual interrupt lockout flag is set and not cleared until control word processing is complete. The message:

CONTROL WORD, PGM NAME

is output on the Standard Output Comment Medium {SOCM}, signaling that the supervisor is ready for control word input.

Control words are input on the Standard Input Comment Medium {SICM} in the following format.

{Control Word}, {Diagnostic Mnemonic Name} (CR)

NOTE: Not all control words require a test mnemonic name. Also, if the operator does not input during the time out period, the TTY or CRT will have a no interrupt error and the message

TTY/I/O ERR 00

will be output.

The legal control words are:

Control Word	Description
CLEAR	Signals to the Diagnostic Supervisor that the condition is not needed. CONTROL WORD, PGM NAME
INDEX	Outputs the Memonic Name of all Diagnostic Routines in core, their address in core and the contents of the flag word and diagnostic revision date.
LIST	Outputs the Mnemonic Name of all Diagnostic Routines on the loading media if that media is mag tape, disk, or diskette.
LOAD	Load the test whose name is in the second field from the loader device. The test must not already be in core.
PARAM	Set the stop to re-enter parameters flag in the test whose name is in the second field. The test must be executing.
PRTSET	Clear the no error printout flag for the test whose name is in the second field. The test must be executing.
PRTSTP	Set the no error printout flag for the test whose name is in the second field. The test must be executing.
RELEAS	Release core allocated to test whose name is in the second field. The test must not be executing or be expecting the RESUME command.
RESUME	Resume execution of the test whose name is in the second field. The test must have the expect resume flag set.
SETRUN	Start execution of the test whose name is in the second field with the SETRUN flag set. The test must be in core, not executing, and not expecting the RESUME command.

Control Word	Description
START	Start execution of the test whose name is in the second field. Same conditions as for SETRUN.
STOP	Stop execution of the test whose name is in the second field. The test must be executing.

Only the last three characters of the control word or diagnostic mnemonic name are used for determining the validity of the control word or the diagnostic mnemonic name. The following paragraphs define in detail the function of each control word.

"CLEAR" CONTROL WORD

Whenever the Diagnostic Supervisor is in a CONTROL WORD, PGM NAME condition (waiting for input) and this condition is unwanted by the user, inputting CLEAR (CR) will cause this condition to be cleared, the manual interrupt lock-out flag is cleared and an exit is made to the dispatcher.

"INDEX" CONTROL WORD

When the control word INDEX is entered, control is transferred to the index routine. This routine will search the program table for any diagnostic routines which are in core. It will output the six character Diagnostic Mnemonic Name, the hexadecimal core address, the contents of the flag word for the diagnostic and the diagnostic revision date. The output will be on the standard list device (automatically the comment device when the list driver is not in core). When the index is complete, control is returned to control word input.

"LOAD" CONTROL WORD

When the control LOAD is entered along with a Diagnostic Mnemonic Name, the routine will try to load the specified diagnostic provided the diagnostic is not already in core. This is determined by searching the program table for the test mnemonic name. Core is also requested for the test routine and its supplemental parts. The following messages are particular to this control word:

ALRDY IN CORE	- Specified routine is already in core.
LOADER NOT RDY	- Loader not ready when trying to read a record.
NO CORE	- Not enough core available to load test.
LOADER I/O ERR XX	- Loader error while trying to read in a diagnostic routine when XX is the error code (See page 3-9)
PGM STACK FULL	- No more room in Program Pointer Table; cannot load test.
PGM NOT IN LOADER	- Specified routine not found on loader medium (Mag Tape and Cartridge Disk only).

If loading is successful, the diagnostic test routine is scheduled in the same manner as the START control word.

"PARAM" CONTROL WORD

When the control word PARAM is entered along with a Diagnostic Mnemonic Name, but '6' in the specified Diagnostic's flag word is set signalling the Diagnostic to stop execution and return to parameter input. The Diagnostic must be in core and have its busy bit set (bit 15). The Diagnostic must clear the PARAM bit.

"PRTSET" CONTROL WORD

When the control word PRTSET is entered along with a Diagnostic Mnemonic Name, bit '7' in the specified Diagnostic's flag word is cleared, signalling to the Diagnostic that error message printout is enabled if it had previously been disabled. The Diagnostic must be in core and have its busy bit set.

"PRTSTP" CONTROL WORD

When the control word PRTSTP is entered along with a Diagnostic Mnemonic Name, bit '7' in the specified Diagnostics's flag word is set signalling to the Diagnostic to bypass error message output as long as the bit is set. The diagnostic must be in core and have its busy bit set.

"RELEAS" CONTROL WORD

When the control word RELEAS is entered along with a Diagnostic Mnemonic Name, the core occupied by the specified diagnostic is released if the Diagnostic is in core and the busy bit is not set. The Diagnostic must not be waiting for the RESUME command. If released, the name of the Diagnostic is cleared from the Program Table.

"RESUME" CONTROL WORD

When the control word RESUME is entered along with a Diagnostic Mnemonic Name, bit '3' of the specified Diagnostic's flag word is set and bit '2' cleared if the Diagnostic is in core, the busy bit is set and the Expect Resume bit, bit 2, is set. A scheduler request is made to the fifth word of the Diagnostic routine (see START routine).

"SETRUN" CONTROL WORD

When the control word SETRUN is entered, along with a Diagnostic Mnemonic Name, bit '1' of the specified Diagnostic's flag word is set, if the Diagnostic is in core and the busy bit is not set. The busy bit is also set and a scheduler request is made to the fifth word of the Diagnostic routine (see START routine).

"START"

When the control word START is entered along with a Diagnostic Mnemonic Name, the Diagnostic busy bit is set and the Diagnostic is scheduled at level 4 at its fifth word if the Diagnostic is in core and the busy bit is not set.

The Diagnostic Supervisor imposes several restrictions on the format of loadable Test Routines.

1. The first five words of the program must be as follows:

Word	Description
0	Characters one and two of Diagnostic Mnemonic Name
1	Characters three and four
2	Characters five and six
3	Revision date as follows: bits 15-12, hexadecimal digit representing the month; bits 11-4, two decimal digits representing the day; bits 3-0, decimal digit increment of the year 1970.
4	Flag word with following bit assignments:

Bit	Description
0	Stop Flag
1	Setrun Flag
2	Expect Resume Flag
3	Resume Flag
4	Not Used
5	Not Used
6	Param Flag
7	No Printout Flag
8 to 14	Not Used
15	Busy Bit

2. Programs must be coded in run anywhere relocatable form.

3. All external references to programs in the same loadable block must be relative.

4. All external references to monitor must be absolute form.

"STOP" CONTROL WORD

When the control word STOP is entered, along with a Diagnostic Mnemonic Name, bit '0" of the specified Diagnostic's flag word is set, signalling the Diagnostic to terminate execution and exit to the dispatcher. The Diagnostic must be in core and have its busy bit set. The Diagnostic must clear the flag word before exiting.

COMMON CONTROL WORD ERROR MESSAGES

Most of the control words listed in the preceding sections have error messages in common when certain criteria is not met. These error messages are as follows:

The error message

NOT IN CORE

is output by the following control word routines when the specified Diagnostic Mnemonic Name cannot be found in the program table. (Note: The program table lists the last three characters of the Diagnostic Mnemonic Name and the core address of all Diagnostic routines loaded into core.)

PARAM
PRTSET
PRTSTP
RELEAS
RESUME
SETRUN
START
STOP

The error message

PROGRAM BUSY

is output by the following control word routines when an attempt is made to start execution of Diagnostic routine which is in core and is already executing (i.e. the Busy set).

SETRUN
START

This message is also output when an attempt is made to release core from a Diagnostic routine which is executing

The error message

PROGRAM NOT BUSY

is output by the following control word routines when an attempt is made to set control bits in the flag word of a Diagnostic routine which is in core but not executing (i.e. Busy bit is not set.).

PARAM
PRTSET
PRTSTP
RESUME
STOP

The error message

CTL WORD NOT EXPECTED

is output when the RESUME control word is entered and the specified Diagnostic routine did not have the expect resume bit set in its flag word {expect resume flag is bit '2' of the flag word}.

The error message

NOT A CTL WORD

is output when a control word is input which cannot be recognized.

After any of the above error messages is output, control is transferred to the control word input routine.

EXAMPLE 1

OPERATOR EXAMPLES

(MI)	Operator Input
CONTROL WORD, PGM NAME	Supervisor Output
LOAD, TSTCDD (CR)	Operator Input
BEGIN 1739 CDD TEST	Test Output
TESTS, BEG SEC, END SEC, RUNS	Test Output
7E,0,5B00,2 (CR)	Operator Input
1739 INT LINE, WES CODE	Test Output
3,181 (CR)	Operator Input
END 1739 CDD TEST 0002 RUNS 0000 ERRORS	Test Output

EXAMPLE 2

(MI)	Operator Input
CONTROL WORD, PGM NAME	Supervisor Output
LOD,TSTCDD (CR)	Operator Input
NOT A CTL WORD	Supervisor Output
CONTROL WORD, PGM NAME	Supervisor Output
START,TSTCDD (CR)	Operator Input
NOT IN CORE	Supervisor Output
CONTROL WORD, PGM NAME	Supervisor Output
LOAD,TSTCDD (CR)	Operator Input
BEGIN 1739 CDD TEST	Test Output
TESTS,BEG SEC, END SEC,RUNS	Test Output
7E,0,5B00,2 (CR)	Operator Input
1739 INT LINE, WES CODE	Test Output
3,181 (CR)	Operator Input
(MI)	Operator Input
CONTROL WORD,PGM NAME	Supervisor Output
LOAD,TSTCDD (CR)	Operator Input
ALRDY IN CORE	Supervisor Output
CONTROL WORD, PGM NAME	Supervisor Output
START,TSTCDD (CR)	Operator Input
PROGRAM BUSY	Supervisor Output
CONTROL WORD, PGM NAME	Supervisor Output
STOP, TSTCDD (CR)	Operator Input
END 1739 CDD TEST, 0000 RUNS, 0000 ERRORS	Test Output
(MI)	Operator Input
CONTROL WORD, PGM NAME	Supervisor Output
STOP,TSTCDD (CR)	Operator Input
PROGRAM NOT BUSY	Supervisor Output
CONTROL WORD, PGM NAME	Supervisor Output
CLEAR (CR)	Operator Input

The following is a list of loader error codes:

00	No interrupt
01	Lost data
02	Alarm
03	Parity error
04	Checksum error
05	External reject
06	Internal reject
07	Pre-read error
10	Non-negative record length
14	Not ready
16	Controller seek error
17	Drive seek error
18	Address error
19	Protect fault
20	Checkword error
34	Data interrupt after Column 80
35	EOP interrupt before Column 80
37	Current word address status error
48	Controller cylinder address status error
49	Drive cylinder address status error
60	ID record format error {disk thread broken}
61	Calculated address exceeds size of cartridge disk pack.
63	Loader not available for loading {test executing on loader device}

PROGRAM NAME CRTSTU

TEST MNEMONIC TSTSTU

PROGRAM FUNCTION

The 1572-1 Sample Timing Unit (STU) Test Routine tests the performance of the Line Synchronized Timer (LST) and the Programmable Sample Rate Generator (SRG). Specifically, test routine determines that the STU enables and disables interrupts properly. A check is made to see that the individual bits of the SRG counter count correctly and a comparison is made of the time bases of the LST and the SRG. The 1572-1 STU (2NNT printed circuit board) must be mounted in a 1750-1 Computer Interface Unit or a 1750-2 Computer Interface Expander connected directly to a 1750-1.

OPERATING INSTRUCTIONS

Once TSTSTU is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows

```
BEGIN 1572-1 STU TEST
TESTS, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

{Field 1}, {Field 2 } (CR)

where: Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

The remaining bits are not used.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the selected test sequence is to be executed. If bit 15 is set, the test is executed until halted by the user.

Next a message is output on the SOCM as follows:

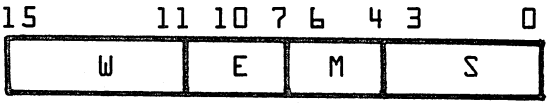
1572-1 INT LINE, WEMS CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

where: Field 1 — the decimal interrupt line number for the 1572-1 Sample Timing Unit must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the STU.



where W = converter code which is normally zero.

E = equipment number of the computer interface unit.

M = module number holding the STU

S = slot number of the STU within the module

The interrupt line input is checked for correct range and if currently busy. If the line is busy but assigned to a system timer, busy condition is accepted. If the line number is not in range or is illegally busy the following message is output on the SICM:

TSTSTU INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

Following correct input of the interrupt line number, a check is made for test 3 or 4 and if requested, the following message is output on the SOCM.

LST INT CNT, MULT, SYNC

Accordingly, the user must enter three control parameters on the SICM in the following format:

{Field 1}, {Field 2}, {Field 3} (CR)

where: Field 1 — 1 to 4 decimal digits representing the number of LST interrupts that will be used to establish the overall time interval for the test.

Field 2 — 1 to 4 hexadecimal digits representing the data that will be loaded into the SRG multiplier register. {This will determine the number of interrupts from the SRG during the time interval established by Field 1}.

Field 3 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit "1" = 1 Enable Sync 1
Bit "2" = 1 Enable Sync 2
Bit "15" = 1 Disable typeout of results.

Upon completion of the number of repeats of the test sequence requested or when halted by the user, the program outputs a message on the SOCM as follows:

END 1572-1 STU TEST, hhhh RUNS hhhh ERRORS

where hhhh is some hexadecimal number.

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

When error conditions are detected, a message is output to describe the error condition. All error messages are preceded by a message segment as follows:

TSTSTU TEST d RUN hhhh

where d is the test section currently executing.

hhhh is the current pass through the test sequence

This message segment is followed by one of the following message segments to complete the description of the error detected.

aaa REJECT Q = hhhh A = hhhh X = hhhh

where aaa is EXT OR INT for the type of reject detected

hhhh is a hexadecimal number

This message means that an extenernal or internal reject has occurred with the Q, A and X register contents as specified by the hexadecimal digits.

aaa ILLEGAL INT, FUNCTION = hhhh

This message means an interrupt was generated by the device defined by aaa {LST or SRG} when the last function word output {hhhh} did not enable that interrupt

aaa NO INT RCVD, FUNCTION = hhhh

This message means an interrupt was not generated by the device defined by aaa {LST or SRG} when the last function word output {hhhh} enabled that interrupt

DATA TO MULT = hhhh DATA FROM CNTR = hhhh

This message means an error was detected between the value output to the multiplier and the data received from the counter after an interrupt was received from the SRG unit. hhhh is the hexadecimal value described by the message. Differences of 8 counts are not detected or counted as errors.

REJECT DURING INT. RESPONSE

This message means an internal or external reject occurred during the interrupt response execution. The current pass through the diagnostic is terminated, and test sequence is restarted.

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input the control parameters which specify the desired test sequence, the number of times to run the test sequence, the 1572-1 interrupt line and the 1572-1 WEMS code. Given these parameters, the program disables the system timer (if the system timer is the 1572-1), releases the system timer interrupt line (if same as one specified for test routine), selects specified interrupt line. A check is made for test 3 and if requested, the additional parameters for that test are requested and input; the user must input: the number of interrupts from the LST to be used as the time base of the test section, the hexadecimal number to be loaded into the SRG multiplier register to control frequency of interrupts from SRG and a control word for the sync signal enables.

The program then proceeds to perform test sections 1, 2, 3 and 4 in order if requested. Each run of test 4 will be preceded by requests for the same defined parameters as test 3.

TEST SECTION 1

This test exercises all function/status of the LST and the SRG. Interrupts are enabled and disabled and a check made on the control of interrupts. Diagnostic messages are output if errors are detected. All functions are left disabled at end of test section.

TEST SECTION 2

Data is transferred to the multiplier register and from the counter of the SRG. The countdown of the individual bits of the counter is verified for the upper 12 bits and count to zero is verified for the lower bits. Differences of less than 8 counts are not detected as errors. All functions are left disabled at end of test section.

TEST SECTION 3

Using the parameters specified before the start of the test sequence, the test will count interrupts from the LST and from the SRG and will type out the results in the following format, if bit 15 of the sync parameter is not set:

TSTSTU TEST 3 RUN hhhh TIME BASE COMP RSLTS
LST INTS dddd SRG INTS dddd

where hhhh is the hexadecimal pass number

dddd is the decimal number of interrupts

The sync signals are enabled as specified by the sync parameter during the execution of this test section. All functions are left disabled at end of test section.

TEST SECTION 4

Each time this test section is entered, the user is requested to input parameters as described in Section 3. The execution of the test section is the same as Test Section 3.

At the conclusion of the number of repeats of the test sequence specified or when the test sequence is halted by the user; the interrupt line is released, and if the 1572-1 was the system timer on the specified interrupt line, the interrupt line is reselected for the system timer and the 1572-1 interrupt is re-enabled. The test then outputs the end messages and terminates.

EXAMPLE: Given: LST input of 60Hz and SRG input of 1000 Hz

```
MI
CONTROL WORD,PGM NAME
START,TSTSTU    CR
BEGIN 1572-1 STU TEST
TESTS,RUNS
E,5    CR
1572-1 INT LINE,WEMS CODE
2,481    CR
LST INT CNT,MULT,SYNC
300,5,0    CR
TSTSTU TEST 3 RUN 0000 TIME BASE COMP RSLTS
LST INTS 0300 SRG INTS 1000 *
TSTSTU TEST 3 RUN 0001 TIME BASE COMP RSLTS
LST INTS 0300 SRG INTS 0999*
TSTSTU TEST 3 RUN 0002 TIME BASE COMP RSLTS
LST INTS 0300 SRG INTS 1000*
TSTSTU TEST 3 RUN 0003 TIME BASE COMP RSLTS
LST INTS 0300 SRG INTS 1000*
TSTSTU TEST 3 RUN 0004 TIME BASE COMP RSLTS
LST INTS 0300 SGG INTS 1000*
END 1572-1 STU TEST, 0005 RUNS, 0000 ERRORS
```

*Due to the non-synchronous nature of the two interrupt sources, a printout of results that shows an SRGINT count that differs by one count from the calculated value is acceptable.

The operator requested that test sections 1, 2 and 3 were to be run. For section 3, theoperator specified that the time base was to be 5 seconds 300 interrupts from the LST, the multiplier value for the SRG was to be 5 (interrupts will occur at a rate of 1000/5 or 200Hz), and the sync outputs are disabled.

PROGRAM NAME CRTAD1, CRTAD2

TEST MNEMONIC TSTAD1, TSTAD2

PROGRAM FUNCTION

This routine tests the performance of 1534 Low-Speed Analog Input Controller. Generally, the routine obtains inputs from a sequence of 1- to 8- channel sets, repeats a specified number of times, compares the actual to the expected counts, and generates a double-precision histogram which allows a maximum count of 9,999,999 for each error counter.

In order to conduct the test, the user must provide the expected full-scale value for each channel being tested. This is most conveniently accomplished using the Analog Input Test Box (Control Data Part No. 39007700) ① which provides variable DC inputs to each channel of a sequence of 8-channel sets. With the test box, the user can apply the desired voltage to each of the channels; then, when requested by the test routine he can enter the full scale reading (%) expected for each channel. This information is converted by the program to expected counts (given that it has previously received correct calibration data). The expected counts are compared to actual counts to produce a histogram of errors.

After each input, checks are made for any error indications returned by the driver. Any errors indicated result in the output of diagnostic messages.

OPERATING INSTRUCTIONS

Once TSTAD1 or TSTAD2 is in control, a message is output on the Standard Output Commend Medium (SOCM) as follows:

```
BEGIN ADC NO. 1 TEST
12 BIT ADC (212-S3-J1)*
BEGIN ADR, END ADR, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of three control parameters in the following format:

(Field 1), (Field 2), (Field 3) CR

*If TSTAD2 -

```
BEGIN ADC NO. 2 TEST
14 BIT ADC (214-S3-J1)
BEGIN ADR, END ADR, RUNS
```

① See Appendix D

Where: Field 1 — 3 hexadecimal digits representing the lowest channel address to be tested.

Field 2 — 3 hexadecimal digits representing the highest channel address to be tested.

Field 3 — 1 to 4 hexadecimal digits representing the number of times each channel is to be multiplexed. If bit 15 is set, the test will execute until a maximum count of 9,999,999 is recorded in any error cell or until halted by the user.

If the ending channel address input is less than the beginning channel address input, the message below is output on the SOCM and the parameters are requested again.

```
TSTAD1 ADR ERR
```

Finally, if zero runs were input or the runs field left blank no message is output but the parameters are requested again.

Next, a message is output on the SOCM as follows:

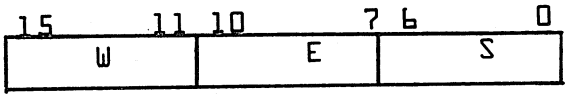
```
1534 INT LINE,WES CODE
```

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

Where: Field 1 — the decimal interrupt line number for the 1534 analog subsystem controller, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1534 controller.



where W = converter code which must always be zero

E = equipment number of the 1750 Date and Control Terminal (DCT)

S = Station address on the 1750 DCT Data and Control Bus (DCB).

The interrupt line input is checked for correct range and whether currently busy. If the line number is not in the range or is currently busy, the following message is output on the SOCM:

TSTAD1 INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

Following correct input of the interrupt line number, a message is output on the SOCM as follows:

SCALE,CK RELAY,DELAY

Accordingly, the user must enter three control words on the SICM in the following format:

{Field 1}, {Field 2}, {Field 3} (CR)

Where: Field 1 — 1 to 4 hexadecimal digits representing the histogram scale factor. The expected counts are subtracted from the actual counts input and the result is divided by a non-zero scale factor to product the scaled conversion error recorded in the histogram.

Field 2 — If the field is non-zero, then whenever the scaled conversion error is greater than +7 or less than -7 a message is output indicating the channel address which was out of range. (see error description page

	Field 3	1 to 4 hexadecimal digits representing the number of 10 millisecond delays to be executed between converting each set of points.

Next, a message is output on the SOCM as follows:

% FS GAIN-SPEED

The user must then enter eight sets of parameters to describe the expected counts and gain for each channel set. The request for each parameter set is preceeded by a message. The message and parameters request are as follows:

POINT X {Field 1} {Field 2} (CR)

Where:	X	The number 1 to 8 for channel sets 1 to 8.
	Field 1	1 to 4 hexadecimal digits representing the expected percent full scale from the channel set. This is a signed value {i.e. if negative, the complement of the percent full is entered}.

Field 2

1 digit representing the amplifier gain for a 1534 channel. The digital is a code which is defined as follows:

Code	1534
0	1 gain
1	10 gain
2	100 gain
3	1000 gain

NOTE: Gains are typical but may vary from system to system. Always lowest gain is Code 0; highest gain is Code 3; for single gain amplifiers, this field can be left blank.

If the expected full scale value is unknown, the user may enter $8000 for Field 1 which signals to the test routine to use the first value input from the channel set as the value for expected counts.

If seven or less channels are requested in the first parameter request, then the channel set information request and the histogram are abbreviated accordingly. (i.e. if 800 and 802 are input for the beginning and ending channel addresses respectively, then channel set information is requested only for points 1, 2 and 3).

EXAMPLE:

```
MI
CONTROL WORD,PGM NAME
START,TSTAD1     CR
BEGIN ADC NO. 1 TEST
12 BIT ADC {212-53-J1}
BEG ADR,END ADR,RUNS
800,807,FFF      CR
1534 INT LINE,WES CODE
8,456     CR
SCALE,CK RELAY,DELAY
1/1/0/    CR
% FS, GAIN, SPEED
```

USER INPUT

```
POINT 1 0,3      CR
POINT 2 0,3
POINT 3 0,3
POINT 4 0,3
POINT 5 0,3
POINT 6 0,3
POINT 7 0,3
POINT 8 0,3      CR
TSTAD1 HISTOGRAM OF RESULTS
SCALE FACTOR 0001 ADDR 0800-0807 RUNS 00004095
```

POINT	1	2	3	4	5	6	7	8
EX CNTS	0000	0000	0000	0000	0000	0000	0000	0000
SP/GAIN	0003	0003	0003	0003	0003	0003	0003	0003
GT	0	0	0	0	0	0	0	0
+7	0	0	0	0	0	0	0	0
+6	0	0	0	0	0	0	0	0
+5	0	0	0	0	0	0	0	0
+4	0	0	0	0	0	0	0	0
+3	0	0	0	0	0	0	0	0
+2	0	0	0	0	0	0	0	0
+1	0	0	0	0	0	0	0	0
0	4095	4095	4095	4095	4095	4095	4095	4095
-1	0	0	0	0	0	0	0	0
-2	0	0	0	0	0	0	0	0
-3	0	0	0	0	0	0	0	0
-4	0	0	0	0	0	0	0	0
-5	0	0	0	0	0	0	0	0
-6	0	0	0	0	0	0	0	0
-7	0	0	0	0	0	0	0	0
LT	0	0	0	0	0	0	0	0

```
END ADC NO. 1 TEST, 0000 ERRORS
```

FIGURE 1. TSTAD1 DOUBLE-PRECISION HISTOGRAM

Upon completion of the number of times each channel was requested to be multiplexed or when halted by the user, the resultant histogram is output (if the SKIP SWITCH is not set) on the Standard List Device (SLD) followed by a message on the SOCM as follows:

END ADC NO. 1 TEST, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then terminates and exits to the dispatcher.

Figure 1, page is an example of the parameter input and resultant histogram.

Error messages output by the program are of one general type as shown below:

TSTAD1 CHNL {1} {2}

where {1} Four-digit hexadecimal channel address

{2} Any one of the following messages.

INT/EXT REJ	Internal or external reject from the 1534 controller or the channel itself.
UNDER RANGE	Channel input is under the range of the A/D converter.
OVER RANGE	Channel input is over the range of the A/D converter.
CK RELAY	Value of the scaled conversion error is outside the range of the histogram (ie. greater than +7 or less than -7). This message is determined by the test and is not counted as an error.

PROGRAM DESCRIPTION

The analog input channels are read in blocks of one to eight channels in sequence until all channels from the beginning address to the ending address are completed. This sequence constitutes one pass and is repeated until the number of passes equals the number specified, the user halts the test, or a histogram table cell overflows, whereupon the histogram table is generated and output along with other information.

Inputs are obtained from each channel in the following manner. The data table used by the Analog Input Driver is filled with a sequence of channel addresses and gain/speed designators, and the input request is executed. When control returns to the test routine each expected count is subtracted from the applicable actual counts; the result is divided by a non-zero scale factor; and a cell designated as a counter for errors of a specific magnitude on one of the eight channels is incremented. If the input count is replaced with an error code, it is processed to output the appropriate diagnostic messages and ignored. The program generates the histogram by processing the tables-of-error counters.

The program allows the user to specify the full-scale voltage (%) to be applied to each channel. That voltage is converted to the equivalent expected counts provided that the user has previously supplied the correct calibration data (i.e., counts equivalent to 0 and 100 percent full-scale readings). If $8000 is input for % full scale, the first data input from CHNL is stored in the counts compare table.

If the SELECTIVE SKIP key is turned on, the test routine will exit without producing the histogram.

SUPPLEMENTAL SOFTWARE

PDTAD1 - 1534 Driver Physical Device Table
ADCDVR - 1534 Driver (12 Bit ADC)
ADCDRV - 1534 Driver (14 Bit ADC)

PROGRAM NAME CRTRL1

TEST MNEMONIC TSTRL1

PROGRAM FUNCTION

This routine tests the performance of the 1558/1559 Latching Relay Subsystem and the 1544 Digital Input Interface. Operation of the test requires that each 1559 channel to be tested be connected to a 1544 channel. (1) Thus, various bit patterns are output on the 1559 and input on the 1544; the digital inputs are compared with the output images. Five types of bit configurations are output to the 1559:

1. $FFFF_{16}$ on one channel; all others 0000_{16}.
2. 0000_{16} on one channel; all others $FFFF_{16}$.
3. User input pattern on one channel; all others 0000_{16}.
4. Left-shifting one bit on one channel; all others 0000_{16}.
5. Left-shifting a zero bit on one channel; all others $FFFF_{16}$.

After each output and input, checks are made for any error indications returned by the drivers. Any errors sensed result in the output of diagnostic messages.

OPERATING INSTRUCTIONS

Once TSTRL1 is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN 1558-1559/1544 TEST
TESTS, SWITCH, RUNS, INDCT WES CODE
```

(1) See Appendix

The program then enables the Standard Input Comment Medium {SICM} for user keyboard input of four control parameters in the following format:

{Field 1},{Field 2},{Field 3},{Field 4} (CR)

where: Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

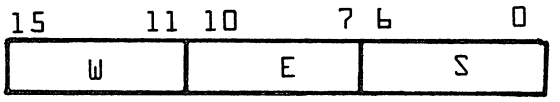
Bit 5 = "1" Do Test 5

The remaining bits are not used.

Field 2 — If non-zero the normally closed contacts are being tested. If zero the normally open contacts are being tested.

Field 3 — 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test will execute until halted by the user.

Field 4 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the '@' register to address the 1750 Data and Control Terminal {DCT} to which the 1544 Digital Input Interface is connected



where W = converter code which must always be zero.

E = equipment number of the 1750 DCT

S = station address of the 1750 DCT, always zero.

Next, a message is output on the SOCM as follows:

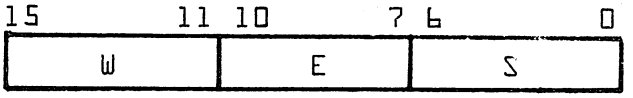
1558 INT LINE, WES Code

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1},{Field 2} (CR)

where: Field 1 — the decimal interrupt line number for the 1558 Latching Relay Subsystem Controller, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the '0' register to address the 1558 controller.



where:
- W = converter code which must always be zero
- E = equipment number of the 1750 DCT
- S = station address on the 1750 DCT Data and Control Bus DCB.

The interrupt line input is checked for correct range and to determine if it is currently busy. If the line number is not in the range or is currently busy, the following message is output on the SOCM:

TSTRL1 INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

Following correct input of the interrupt line number, a message is output on the SOCM as follows:

OUT CHNL,IN CHNL

Accordingly, the user must input on the SICM the channel connection information. Each channel set is input separately as shown below:

{Field 1},{Field 2} (CR)

{Field 1},{Field 2} (CR)

. . .

{Field 1},{Field 2} (CR)

FFFF (CR)

Where:

Field 1	0 to 2 hexadecimal digits representing an allowable 1559 channel address.
Field 2	0 to 2 hexadecimal digits representing an allowable 1544 channel address.
FFFF	Input for Field 1 when the user has specified all channel combinations to be tested. A maximum of 16 combinations can be tested at one time.

Upon completion of the number of repeats of the test sequence requested or when halted by the user, the program outputs a message on the SOCM as follows:

END 1558-1559/1544 TEST, hhhh RUNS, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then terminates and exits to the dispatcher.

If test 3 was requested the test halts, before beginning the test sequence, for the user to input the special test pattern as follows:

ENTER SPECIAL PATTERN FOR TEST 3

The message above is output on the SOCM and the user must input one parameter as follows:

{Field 1} (CR)

Where: Field 1 — 1 to 4 hexadecimal digits representing the special test pattern.

ERROR MESSAGE DESCRIPTION

Two types of error messages are output by the program: one for hardware malfunctions and one for discrepancies found between the image output and the image input.

Device reject errors are indicated by a message in the following form:

TSTRL1 TEST {1} RUN {2} {3} aaa {4} {5}

where:

{1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} If 1559 or 1544 aaa = CHL

If 1750 or 1558 aaa = STN

{4} If aaa = CHL, the four digit hexadecimal channel address

If aaa = STN, the four digit hexadecimal station address {WES CODE}.

{5} Error description

1544

INT REJ — Internal reject-no response from unit

EXT REJ — External reject-unit not ready. Most likely caused by the presence of a synchronization device in the unit.

1559

SELECT ERROR — 1559 channel address does not Exist.

1558

TIME OUT — No interrupt in the time period allowed {requires System Timer}

BUSY — Controller still busy after interrupt.

INT REJ Internal reject - no response from unit.

EXT REJ External reject - unit busy {output}.

1750

INT REJ Internal reject-no response from unit.

EXT REJ External reject-unit not ready {check protect switch}.

When device errors are detected, no data compare is done.

Whenever the image input differs from the image output, the following message is output:

TSTRL1 TEST {1} RUN {2} OUT CHNL {3} IS {4} IN CHNL {5} IS {6}.

where: {1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} Four-digit hexadecimal 1559 channel address.

{4} Four-digit hexadecimal image output.

{5} Four-digit hexadecimal 1544 channel address.

{6} Four-digit hexadecimal image input.

Both type of error messages are output on the Standard List Device {SLD}.

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input the control words and the pair of connected channels. Upon completion of this input, each of the specified tests is conducted in sequence.

Generally, each test involves generating some bit configuration for output on a 1559 channel. A time delay of 8 milliseconds is executed after each output. When the output is accomplished; a check is made for any reject error indications returned by the dirver; a digital input is accomplished on the connected 1544 channel; and a check is made for any reject error indications returned by the 1544 driver. The digital input is compared with the image output; any differences will result in a diagnostic message.

The specific structure of each test is as follows:

TEST SECTION 1

All output relays are zeroed. The image $FFFF_{16}$ is output to a channel. Digital inputs are read from all channels and the inputs are compared to the output images. This procedure is repeated for all channels specified.

TEST SECTION 2

All output relays are set to $FFFF_{16}$. A channel is zeroed. Digital inputs are read on all channels and the inputs are compared to the output images. This procedure is repeated for all channels specified.

TEST SECTION 3

All output relays are zeroed. The special pattern input by the user is output on each channel as in Test 1.

TEST SECTION 4

All output channels are zeroed. Taking each channel in turn, a bit is left-shifted sequentially from positions 0 through 15. The image is output after each shift of the bit, digital inputs are read on all channels, and the inputs are compared to the output images. Each channel is again zeroed once bit 15 has been set and output/input accomplished. This procedure is repeated for each channel specified.

All output relays are set to ones, and the above procedure is repeated with a zero bit being shifted and each channel reset to $FFFF_{16}$ when it is completed.

TEST SECTION 5

This test is identical to Test 4 with the exception that the current image for each 1559 channel is output after each bit shift in a sequence beginning with the channel being modified.

Current version allows exercise of only 16 channel combinations. However, various internal tables can be expanded as desired.

SUPPLEMENTAL SOFTWARE

PDTRL1
CRMLRD
CRMDID

EXAMPLE:

Given: 1558 station address 48 connected to a 1750 with equipment code of 8 1558 interrupt line is 9. There are four 1559 channels, channel addresses 080, 081, 082 and 083. There are four 1544 channels 000, 001, 002 and 003 which are connected to a 1750 with equipment code of 9. The channels are cabled together via the digital input test box as follows:

Cable from 1544 jack J01 to test box No. 1 jack AI. Cable from 1544 jack J02 to test box No. 2 jack AI. Cable from 1559 jack J07 to test box No. 1 jack A0. Cable from 1559 jack J08 to test box No. 1 jack B0. Cable from 1559 jack J09 to test box No. 2 Jack A0. Cable from 1559 jack J10 to test box No. 2 jack B0.

Cable from 1544 to test box is P/N 389203XX.
Cable from 1559 to test box is P/N 389177XX.

All test sections will be run for 10_{16} times, testing the normally open contacts of the relays. Section 3 will use the pattern 1234_{16} for the special pattern.

```
MI
CONTROL WORD, PGM NAME
START, TSTRL1     CR
BEGIN 1558-1559/1544 TEST
TESTS,SWITCH, RUNS,IN DET WES CODE
3E,0,10,480   CR
1558 INT LINE,WES CODE
9,448     CR
OUT CHNL,IN CHNL
80,00   CR
81,01
82,02
83,03
FFFF    CR
ENTER SPECIAL PATTERN FOR TEST 3
1234    CR
TSTRL1 TEST 1 RUN 0008 1544 CHL 0002 EXT REJ
TSTRL1 TEST 5 RUN 000F 1559 CHL 0080 SELECT ERROR
END 1558-1559/1544 TEST, 0010 RUNS 0002 ERRORS
```

PROGRAM NAME

CRTCRT

MNEMONIC NAME

TSTCRT

PROGRAM FUNCTION

The 1595-1X Serial Input/Output card/713-10 or OEM 92423 (QSE) Cathode Ray Tube Display Test Routine tests the performance of the afore mentioned units by outputting the allowable character set for the 713-10 CRT display. This requires the operator to verify the correctness of the characters output. The test has three sections as follows:

1. Allowable character ripple pattern test.

2. Echo test.

3. User pattern output test.

In all three tests, the user must verify the correctness of the output characters as there is no feedback from the CRT. The 1595-10/11 SIO (T printed circuit card) must be mounted in a 1750 Computer Interface Unit or a 1750-2 Computer Interface Expander connected directly to a 1750-1.

OPERATING INSTRUCTIONS

Once TSTCRT is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN 1595 SIO/713 CRT TEST
TEST,RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format :

(Field 1),(Field 2) (CR)

where Field 1 — 1 to 4 hexidecimal digits representing 16 bits with the following assignments

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

The remaining bits are not used.

Field 2 — 1 to 4 hexidecimal digits representing the number of times the selected test section is to be executed. If bit 15 is set, the test section will be executed until halted by the user.

Next, a message is output on the SOCM as follows:

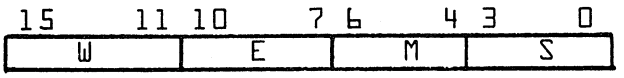
1595 INT LINE, WEMS CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1},{Field 2} (CR)

where Field 1 — the decimal interrupt line number for the 1595 Serial Input/Output card {SIO}, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexidecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1595 SIO card.



where: W = converter code which is normally zero.

E = equipment number of the computer interface unit.

M = module number holding the 1595 SIO

S = slot number of the 1595 SIO within the module

The interrupt line input is checked for correct range and if currently busy. If the interrupt line is not in range or is currently busy, the following message is output on the SOCM:

TSTCRT INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

Following correct input of the interrupt line number and equipment address, the test section selected begins execution.

Upon completion of the number of repeats of the test section selected or when halted by the user, the program outputs a message and the SOCM as follows:

END 1595/713 TEST, hhhh RUNS hhhh ERRORS

where hhhh is some hexidecimal number.

The program then terminates and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

All error messages are output on the Standard List Device {SLD} and are of the same general format as shown below:

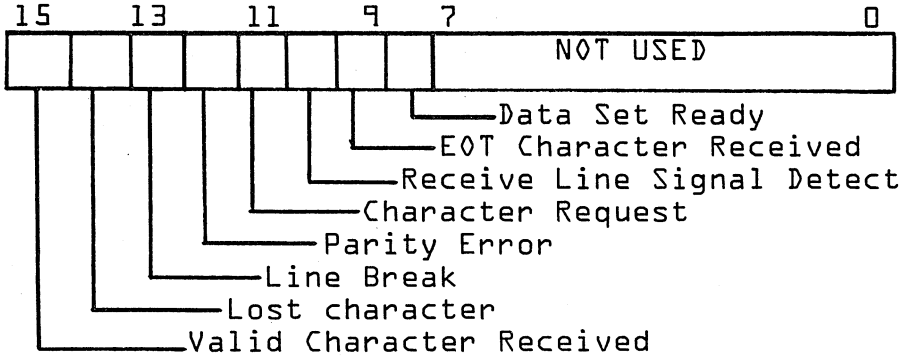
TSTCRT RUN {1} {2} STATUS = {3}

where {1} hexidecimal number of the current pass through the test section requested.

{2} One of the following messages

TIME OUT	No interrupt received during driver limit.
PARITY	Incorrect character parity on input from display unit
ALARM	Lost Data or Line Break
INT REJ	Internal reject {status message is eliminated}, no response from unit
EXT REJ	External reject.

{3} Hexidecimal number indicating the last status from the SIO card. The status is defined as follows:



PROGRAM DESCRIPTION

Once the test is loaded, the physical device table is absolutized before the title message is output. Before the test executes, the user must input the test section to be executed, the number of times to execute the test section, the 1595 interrupt line and the 1595 WEMS code. Before the execution starts on the selected test section, the interrupt line assignment is requested and the logical unit tables are set up after a logical unit is assigned.

TEST SECTION 1 -

The test outputs a line of 79 characters composed of the allowable character set (96) in numerical order (i.e. ASCII order). The buffer is then left shifted one character and the next consecutive character is added at the end. This new line is then output. One pass through the test consists of outputting every character in every character position on the line.

TEST SECTION 2 -

The test outputs the message INPUT CHARACTER STRING in an inverse video field. The user should input a string of allowable characters followed by a Carriage Return (CR). The number of characters input is limited to 80. The driver is monitored by the diagnostic clock (if operational), therefore the user must enter a character every two minutes to avoid a TIME OUT error. If a Time Out occurs, the current contents of the SIO buffer is output. When the user enters a (CR), the test routine then outputs the data it received from the display unit and requests input again.

TEST SECTION 3 -

The test requests and inputs as in Test 2 but the character string input is then continuously output to the CRT screen for the number of times requested in the RUN parameter.

Each input and output to the CRT display is checked for hardware detectable errors. Diagnostics messages are output if any error exists.

Each test section starts by outputting a clear screen function character.

SUPPLEMENTAL SOFTWARE

SIOCRT IOM 1595 Driver
IN1595 Interrupt REsponse Routine
PDTCRT Physical Device Table

EXAMPLE

```
MI
CONTROL WORD,PGM NAME
LOAD,TSTCRT
BEGIN 1595 SIO/713 CRT TEST
TEST,RUNS
2,10    CR
1595 INT LINE, WEMS CODE
14,48C    CR
END 1595/7B TEST, 0001 RUNS 0000 ERRORS


MI
CONTROL WORD,PGM NAME
START,TSTCRT
BEGIN 1595 SIO/713 CRT TEST
TEST,RUNS
2,8000    CR
1595 INT LINE,WES CODE
14,48C    CR
TSTCRT RUN 0032 TIME OUT STATUS = 8000
TSTCRT RUN 0157 TIMEOUT STATUS = 0000
MI
CONTROL WORD,PGM NAME
STOP,TSTCRT    CR
END 1595/713 TEST, 0241 RUNS 0002 ERRORS
```

PROGRAM NAME CRTSAU

TEST MNEMONIC TSTSAU

PROGRAM FUNCTION

This routine tests the performance of the 1576-1, -2 Stall Alarm Unit (SAU). Specifically, the test routine determines that the SAU reacts properly to function commands, returns correct status, causes stall interrupts at each of the four levels, allows the operator to create power failures and field stall inputs to check for correct operation. The 1576-1, -2 SAU (3UMT printed circuit board*) must be mounted in a 1750-1 Computer Interface Unit or a 1750-2 Computer Interface Exapnder connected directly to a 1750-1.

OPERATING INSTRUCTIONS

Once TSTSAU is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

BEGIN 1576-X STALL ALARM TEST
TESTS, RUNS, JUMPER

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of three control parameters in the following format:

(Field 1), (Field 2), (Field 3) (CR)

where: Field 1 — 1 to 4 hexadecimal digits representing 16-bits with the following assignments.

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

The remaining bits are not used.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the selected test sequence is to be executed. If Bit 15 is set, the test is executed until halted by the user.

*1576-2 also includes a Stall Alarm Panel.

Field 3 = 0 if the nut and bolt jumper "G-I" used for timer rate selection is not in place.

= 1 if the nut and bolt jumper "G-I" is in place.

Next a message is output on the SOCM as follows:

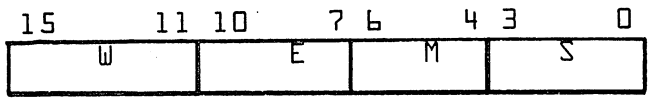
1576-X INT LINE, WEMS CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

where: Field 1 the decimal interrupt line number for the 1576-1, -2 Stall Alarm Unit must be in the range of 2 to 15.

Field 2 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the SAU.



where W = converter code which must equal zero.

E = equipment number of the Computer Interface Unit.

M = module number holding the SAU.

S = slot number of the SAU within the module.

The interrupt line input is checked for correct range and to determine if it is currently busy. If the line number is not in range or is currently busy, the following message is output on the SOCM:

TSTSAU INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

When the interrupt line and WEMS code is input without error the execution of the test sequence is begun.

Upon completion of the number of repeats of the test sequence requested or when halted by the user, the program outputs a message on the SOCM as follows:

```
END 1576-X STALL ALARM TEST, hhhh RUNS
hhhh ERRORS
```

where hhhh is some hexadecimal number.

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

When error conditions are detected, a message is output on the Standard List Device (SLD) to describe error condition.

All inputs and output to the SAU are checked for rejects. When rejects are detected, the following message is output to describe the I/O operation in process at the moment including the appropriate registers. When a reject occurs, the current pass through the test sequence is terminated and the next pass is started.

```
TSTSAU TEST d RUN hhhh
iii REJECT Q = qqqq A = aaaa X = xxxx
```

where

d	test section currently executing
rrrr	current pass through the test sequence.
iii	EXT for external reject. INT for internal reject.
qqqq	contents of the "Q" register at the time of the I/O operation (hardware address).
aaaa	contents of the "A" register (function to be output; zero if input).
xxxx	content of the "X" register (type of I/O operation).

When a status error is detected when checking the SAU Interface the following message is output.

```
TSTSAU TEST 1 RUN rrrr
FUNCTN ffff STATUS ERR. ACTUAL aaaa
EXPECTED eeee
```

where	rrrr	current pass through the test sequence.
	ffff	function output just prior to status check
	aaaa	actual status received from SAU
	eeee	expected status from SAU

See Figures 8.1 and 8.2.

When an error is detected while checking the counting of the four levels of timers, the following message is output.

```
TSTSAU TEST 2 RUN rrrr
COUNTER d COUNT ERR. ACTUAL aaaa
EXPECTED eeee
```

where	rrrr	current pass through the test sequence
	d	counter in error
	aaaa	actual number of overflows detected
	eeee	expected number of overflows

When no stall interrupt is detected when a stall condition should have occurred, the following message is output.

```
TSTSAU NO STALL INTERRUPT
```

No further checks are made for stall interrupts during the current pass through the test sequence.

When no power failure interrupt is detected when the operator was instructed to create the power failure condition, the following message is output.

TSTSAU NO POWER FAIL INTERRUPT

The status of the stall alarm unit is checked for power fail status whether or not an interrupt occurred. If the power fail status is not present, the following message is output.

TSTSAU NO POWER FAIL STATUS

When no field stall interrupt is detected when the operator was instructed to create the field stall condition, the following message is output.

TSTSAU NO FIELD STALL INTERRUPT

The status of the stall alarm unit is checked for field stall status whether or not an interrupt occurred. If the field stall status is not present, the following message is output.

TSTSAU NO FIELD STALL STATUS

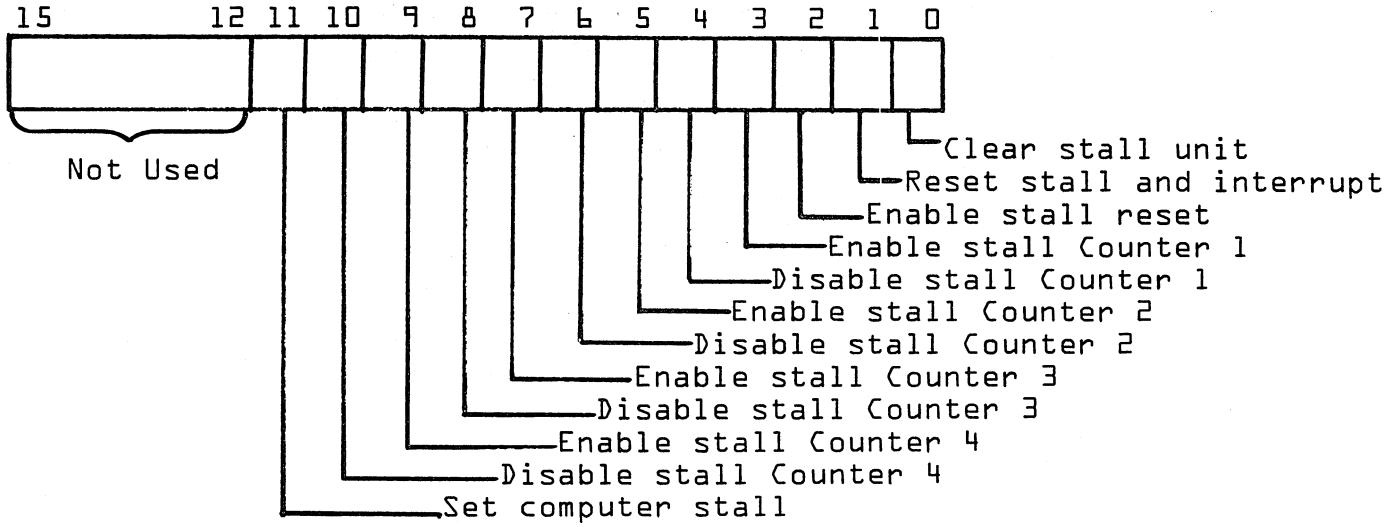


Figure 8.1 SAU Function Word

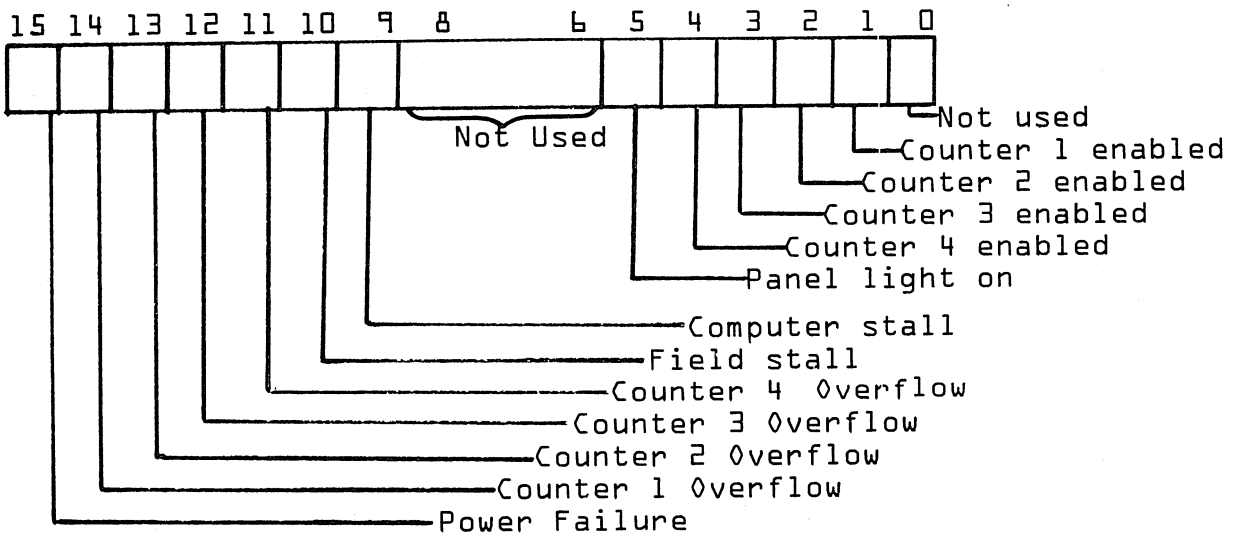


Figure 8.2 SAU Status Word

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input the control parameters which specify the desired test sequence, the number of times to run the test sequence, the condition of the time rate nut/bolt jumper G-I, the 1576-X interrupt line and the 1576-X WEMS code. The program then proceeds to conduct the test sections 1, 2, 3 and 4 in order if requested.

TEST SECTION 1

This section exercises all function/status of the SAU except interrupts. Each function is output and the status input. The status input is checked against the expected status, any deviations detected are reported as errors. The stall alarm unit is left cleared at end of test section.

TEST SECTION 2

This section checks the stall interrupts. First, the counter four is checked to determine whether an overflow condition occurs. If this condition occurs and an interrupt is received, the test section continues. All four counters are enabled and counter 4 is used as a time base for the other 3 counters. The time duration is 60 seconds and is corrected according to the jumper G-I. The counters are then checked against the expected value, any deviations are reported as errors. It should be noted that errors in Counters 1,2 and 3 may be caused by an error in Counter 4. Also, if a field stall or power failure is detected during this test, the test section will be terminated immediately; this will probably cause count errors on all counters.

TEST SECTION 3

This test section requires operator interaction to run successfully. The power fail interrupt capability of the stall alarm is tested by the operator removing the power from the line monitoring input to the stall alarm. The test outputs the following message to alert the operator to create the test condition.

```
TSTSAU TEMPORARILY INTERRUPT POWER
 AT STALL ALARM
```

The operator then has 30 seconds to create a power fail condition. Please Note: All power to the 1750-X should not be interrupted, only the power to the line monitoring transformer , or remove stall power plug (Pins A16, A17, B16, B17) on back-plane of module at slot address.

The test will wait for 30 seconds or until the power fail interrupt is detected, whichever is shorter. At the interrupt or at the time out, the status of the stall alarm unit is checked for status conditions. Any condition not as expected is reported as an error.

The operator is then notified to restore power to stall alarm by the following message.

TSTSAU RESTORE POWER TO STALL ALARM

This message is repeated every 10 seconds until the power fail condition is no longer detected.

TEST SECTION 4

This test section also requires operator interaction to run successfully. The field stall interrupt capability of the stall alarm is tested by the operator creating a field stall input. The test outputs the following message to alert the operator to create the test condition.

TSTSAU SET FIELD STALL INPUT

The operator then has 30 seconds to create a field stall input, by grounding Pin B19 on backplane of module at slot address, or set field stall at stall panel.

The test will wait 30 seconds or until the interrupt occurs, whichever is shorter. In either case, the status is checked for proper condition; any deviation is reported as an error.

At the end of the test sequence (to here if a reject occurred) a pass counter is updated and checked against the number of repeats specified. At the conclusion of the number of repeats specified or when halted by the user, the test outputs the end message on the SOCM and terminates.

Each test section releases the interrupt line at its conclusion.

The user should be aware that the test causes stall conditions to occur which therefore send the STALL signal to all 1750-X slot positions. Any units expecting this signal will act accordingly.

EXAMPLE

Given: SAU in Slot 5 of 1750-1 CIU with equipment number 8. SAU jumper G-I is in place. Interrupt line 15 is used for SAU.

```
(MI)
CONTROL WORD, PGM NAME
LOAD, TSTSAU      (CR)
BEGIN 1576-X STALL ALARM TEST
TESTS, RUNS, JUMPER
1E, 1, 1          (CR)
1576-X INT LINE, WEMS CODE
15, 485           (CR)
TSTSAU TEMPORARILY INTERRUPT POWER AT STALL ALARM
TSTSAU RESTORE POWER TO STALL ALARM
TSTSAU RESTORE POWER TO STALL ALARM
TSTSAU RESTORE POWER TO STALL ALARM
TSTSAU SET FIELD STALL INPUT
END 1576-X STALL ALARM TEST, 0001 RUNS, 0000 ERRORS
```

```
(MI)
CONTROL WORD, PGM NAME
START, TSTSAU     (CR)
BEGIN 1576-X STALL ALARM TEST
TESTS, RUNS, JUMPER
8, 1,1            (CR)
1576-X INT LINE, WEMS CODE
15, 485           (CR)
TSTSAU TEMPORARILY INTERRUPT POWER AT STALL ALARM
TSTSAU NO POWER FAIL INTERRUPT
TSTSAU NO POWER FAIL STATUS
TSTSAU RESTORE POWER TO STALL ALARM
END 1576-X STALL ALARM TEST, 0001 RUNS, 0002 ERRORS
```

PROGRAM NAME CRTCDD

MNEMONIC NAME TSTCDD

PROGRAM FUNCTION

The 1739-1 Test Routine is a series of tests designed to exercise and determine the performance of the 1739-1 Disk Controller and Drives in its various modes of operation using the operating system disk driver. The user must specify the dimensions of the disk section to be tested and the particular operations to be performed as part of the test sequence. The program exercises and diagnoses the performance of the following operations:

1. Read/Write head switching.
2. Core-to-disk transfers of information (1) in block lengths 2048_{10} words.
3. Disk-to-core transfers of information (1) in block lengths 2048_{10} words.
4. Transfer of information from a specified core/disk location to a specified disk/core location.
5. Read head positioning (seek operation).

Any errors sensed during the conduct of a test will cause appropriate diagnostics to be output on the Standard List Device (SLD). The program will diagnose any of the following discrepancies:

1. Alteration of information during core-to-disk or disk-to-core transfers.
2. Transferred information displaced from destination locations.

---

(1) Information includes four worst patterns (#9555, #6AAA, #5A5A and #A5A5), all ones, and pseudo-random bit patterns.

3. Lost data, address, seek, defective track and storage parity errors during write operation.

4. Lost data, address, seek, protect fault, defective track, check word and storage parity errors during read operation.

OPERATING INSTRUCTIONS

Once TSTCDD is in control, a message is output on the Standard Output Commend Medium (SOCM) as follows:

```
BEGIN 1739 CDD TEST
TESTS, BEG SEC, END SEC, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of our control words in the following format.

(Field 1),(Field 2),(Field 3),(Field 4) (CR)

where:

Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

Bit 5 = "1" Do Test 5

Bit 6 = "1" Do Test 6

The remaining bits are not assigned.

Field 2 — 1 to 4 hexadecimal digits representing the disk sector address at the beginning of test area.

Field 3 — 1 to 4 hexadecimal digits representing the disk sector address at the end of test area.

Field 4 — 1 to 4 hexadecimal digits representing number of times the test sequence is to be run. If bit 15 is set, the test will execute until halted by the user.

If the beginning disk address is larger than the ending disk address or the ending disk address exceeds the size of the disk, the message below is output on the SOCM and the parameters are requested again.

```
TSTCDD SEC ADD ERR
```

Next, a message is output on the SOCM as follows:

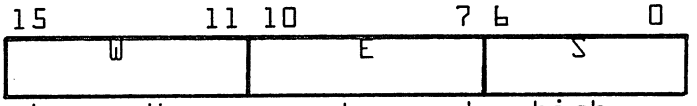
```
1739-1 INT LINE, WES CODE
```

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

where Field 1 — the decimal interrupt line number for the 1739-1 controller, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits loaded into the 'Q' register to address the 1739-1 controller as shown below:



where: W = converter code which must be zero.

E = equipment number of the 1739-1 controller.

S = station address for level one status - always equal to 1.

The interrupt line input is checked for correct range and if currently busy {in use}. If the line number is not in range or is currently busy, the following message is output on the SOCM:

```
TSTCDD INTERRUPT ASSIGNMENT ERROR
```

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

Following correct input of the interrupt line number, the test sequence is begun.

Upon completion of the number of repeats of the test sequence requested or when halted by the user, a message is output on the SOCM as follows:

END 1739 CDD TEST, hhhh RUNS, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

All error messages output by the program are output on the Standard List Device (SLD) and are of the same general format as shown below:

TEST (1) RUN (2) (3) (4) XFER H/W ADDR. (5)

where: (1) Decimal number of the test currently being executed

(2) Hexadecimal number of the current pass through the test sequence.

(3) One of the following error messages:

NOT RDY — Disk unit not ready. Can also result from a reject

COMP ERR — Data comparison error. An additional message is also output describing the location and actual data error. (The direction of transfer is deleted from this message).

LOST DATA — A second word was received from the drive unit before the first word was transferred to core and then an attempt was made to transfer a word to core.

PARITY — Core storage parity error detected during data transfer.

PROTECT — A data transfer was initiated from unprotected core to or from a protected area.

ADR ERR — An illegal disk address was received by the controller.

DRIVE SEEK ERROR — Drive unit detected a seek error.

CONTROLLER SEEK ERROR — 1739-1 controller detected a seek error condition.

TIME OUT — 1739-1 controller did not interrupt when expected.

NO COMP — Error detected during a hardware data compare operation. Should never be output as driver does not perform this operation.

CHKWRD ERR — Checkword on disk pack does not equal that calculated by the controller during data transfer.

INT REJ — Internal reject was received. 1739-1 did not respond to I/O command.

EXT REJ — External reject was received. 1739-1 sent a reject to an I/O command.

REG. STATUS ERROR — One of the following registers did not agree with what was expected:

CURRENT WORD ADDRESS
CONTROLLER CYLINDER ADDRESS
DRIVE CYLINDER ADDRESS

An additional message is output to describe the complete error {See description below}.

{4} Direction of transfer

D-C — Disk to core
C-D — Core to disk

{5} Actual disk hardware address {hexadecimal} at the beginning of the data transfer.

In the case of a comparison error {COMP ERR}, additional messages are output in the following format:

WORD {1} WAS {2} IS {3}

where: {1} Hexadecimal number of the word within the sector where the contents were altered.

{2} Bit pattern sent to that word.

{3} Bit pattern returned from that word.

When the comparison test has been completed and at least one or more comparison errors were detected, a message is output on the SLD as follows:

TSTCDD COMP ERR TOTAL {1}

where: {1} Hexadecimal total of comparison errors detected in the block being tested {range 1 - 800}.

In the case of a register status error {REG. STATUS ERROR} an additional message is output on the SLD following the first error message. The format is:

{1} ADDRESS STATUS-ACTUAL {2} EXPECTED {3}

where {1} is one of the following:

CURR WORD for a current word address register error

CNTLR CYL for a controller cylinder address register error

DRIVE CYL for a drive cylinder address register error

{2} The actual register contents

{3} The expected register contents

A typical error printout would be as follows:

```
TSTCDD TEST 4 RUN 0013 PARITY D-C XFER
  H/W ADR. 0104
TSTCDD TEST 4 RUN 0013 COMP ERR H/W ADR. 0104
WORD 0020 WAS B5A2 IS B1A2
TSTCDD COMP ERR TOTAL 0001
TSTCDD TEST 4 RUN 0013 REG. STATUS ERROR D-C
 XFER H/W ADR. 0104
CURR WORD ADDRESS STATUS-ACTUAL 2F42
 EXPECTED 2F5B
```

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input six control words which specify the desired test sequence, the beginning sector address, the ending sector address, the number of times to repeat the test sequence, the controller interrupt line number and the controller WES code.

The test addresses the disk as a word addressable device (2-word address as in the 1751 Drum) instead of sector addressable (96 words/sector). Accordingly, the sector addresses are initially converted to two-word addresses which are used throughout the test. When an error is encountered, the current two-word address is converted to a hardware address (as is output to the disk controller for a load address function) plus some word number if appropriate. The resultant addresses are output in the diagnostic message.

The program jumps to each of the tests (See pages 9-8,9-9) desired by the user and outputs appropriate diagnostic messages when errors are detected. The following procedures are common to each test.

Information to be written on the disk is loaded into a fixed 2048_{10} word buffer. The variable parameters of the disk transfer call sequence are specified, and a Monitor request is executed to accomplish the transfer of the specified number of words to the specified disk area. The beginning core address for the transfer is fixed for all tests. The block of information generated for a particular test is repeatedly transferred until it has been written throughout the specified disk test area. Once this has been accomplished each block of information is read from the disk into the buffer, and the original information if regenerated and compared to that contained in the buffer. Any discrepancy between the original information and that returned from the disk results in the output of a comparison error message on the SLD.

At the completion of each transfer request, the status returned by the disk is examined for any error bits set. Any error condition results in the output of a diagnostic message that indicates the actual h/w address at which the transfer began. Any error condition will cause the transfer to be repeated once. In the case of a parity error, a comparison check is made prior to the re-execution of the transfer. (Note: the comparison check is <u>not</u> executed if the parity error occured while conducting Test 4. The transfer is, however, re-attempted.)

Upon completion of the second transfer, the program checks the disk status, outputs diagnostic messages if any errors still exist, and resumes the normal sequence. At this point, all tests conduct a comparison check. The comparison test of the original patterns and the returned patterns is conducted throughout each transferred block even though comparison errors exist throughout the block. Comparison error messages are suppressed after the third error in a block; a tally of comparison errors for that block is computed and printed out when the comparison test is completed but only when at least one or more comparison errors were sensed in that block.

When the program completes a pass through all specified tests, it determines whether or not the test sequence should be terminated either because the test sequence has repeated the specified number of times or because the user has set the stop flag (i.e. STOP/TSTCDD). Also, the stop flag is checked after each disk transfer.

TEST SECTION 1

Transfer 2048_{10} Word Blocks of Worst Bit Patterns

Four worst patterns are used in this test: 9555_{16}, $6AAA_{16}$, $5A5A_{16}$, and $A5A5_{16}$. The 2048_{10} word buffer is loaded with a worst pattern and transferred to the disk until it is completely loaded. The disk is read a block at a time, and each word of the 2048_{10} word block is compared with the original pattern. This procedure is repeated for each of the four worst patterns.

TEST SECTION 2

Transfer 2048_{10} Word Blocks Containing all Ones

The 2048_{10} word buffer is filled with "1's" and transferred to the disk until it is completely loaded. The disk is read a block at a time, and each block of information is checked for all "1's."

TEST SECTION 3

Transfer 2048_{10} Word Blocks of Pseudo-Random Bit Patterns

The 2048_{10} word buffer is filled with randomly generated bit patterns and repeatedly transferred to the disk until it is completely loaded. Each block is read and compared with the original information a block at a time. A new set of random numbers is generated for each pass through this block.

TEST SECTION 4

Transfer Pseudo-Random-Length Blocks of Pseudo-Random Bit Patterns

The 2048_{10} word buffer is loaded with randomly generated bit patterns; then, successive block lengths are randomly generated, and a block is transferred for each length generated. The blocks are written on the disk so that each block begins directly following the succeeding one. When the test is completed, the random information is read a block at a time and compared with the original patterns. A new set of random patterns and random block lengths are generated for each pass through this test.

TEST SECTION 5

Transfer 2048_{10} Word Blocks Containing All Ones

The 2048_{10} word buffer is filled with "1's" and transferred to the disk until it is completely loaded. This phase is repeated ten times. The buffer is zeroed and transferred to the disk until it is completely loaded. The disk is read a track at a time, and each block is checked for all zeros.

TEST SECTION 6

Transfer 2048_{10} Word Blocks Containing Worst Pattern 9555_{16} to Random Addresses

The 2048_{10} word buffer is filled with the worst pattern 9555_{16}. The block is then transferred to and read from the disk at randomly generated addresses. Each block is checked for 9555_{16} throughout.

NOTES:

To convert to or from sector addressing to hardware addressing, the following should be remembered:

```
 96 words (16 bit) per sector
 29 sectors per track
  2 tracks per cylinder
203 cylinders per disk
  2 disks per drive
```

Normally, Disk 0 is the removable disk and disk 1 is the fixed disk.

The test routine considers the drive with two disks as one continuous medium.

There are 11774_{10} sectors on a disk therefore, the highest sector address on disk 0 is $2DFD_{16}$, the lowest sector address on disk 1 is $2DFE_{16}$ and the highest sector address on disk 1 is $5BFB_{16}$.

Run time (approximate) for all disk sectors, all test sections is 3-1/2 hours.

SUPPLEMENTAL SOFTWARE

PDTCDD Physical Device Table for D1739Q
D1739Q Modified MSOS 4.1 1739-1 Driver D1739I

EXAMPLE

Given: 1739-1 CDD with both disks on the drive unit Controller has an equipment code of 3 and an interrupt line of 3.

```
(AI)
CONTROL WORD, PGM NAME
LOAD, TSTCDD                (CR)
BEGIN 1739 CDD TEST
TESTS, BEG SEC, END SEC, RUNS
7E, 0, 5BFB, 2              (CR)
1739-1 INT LINE, WES CODE
3, 181  (CR)
END 1739 CDD TEST, 0002 RUNS 0000 ERRORS
(MI)
CONTROL WORD, PGM NAME
START, TSTCDD    (CR)
BEGIN 1739 CDD TEST
TESTS, BEG SEC, END SEC, RUNS
40, 0, 2DFD, 1    (CR)
1739-1 INT LINE, WES CODE
3, 181     (CR)
TSTCDD TEST 6 RUN 0000 COMP ERR H/W ADR 0104
WORD 0020 WAS 9555 IS 0000
TSTCDD TEST 6 RUN 0000 COMP ERR H/W ADR 0104
WORD 0025 WAS 9555 IS 0000
TSTCDD COMP ERR TOTAL 0002
END 1739 CDD TEST, 0001 RUNS 0002 ERRORS
```

PROGRAM NAME CRTDIO

TEST MNEMONIC TSTDIO

PROGRAM FUNCTION

This routine tests the performance of the IOM 1553-X Digital Output Unit (DOU) and the IOM 1544-X Digital Input Unit (DIU). Operation of the test requires that each 1553-X card be cabled to a 1544-X card (for test purposes, the 1553-X card and 1544-X card can occupy the same slot position). Cross reference of units tested by the routine is as follows:

Product No.	Equip. No.	Part No.	Card Type
1544-1	DA101B	39842201	2NRT
1544-2	DA101A	39842200	1NKT
1544-3	DA401B	39842203	2NTT
1544-4	DA401A	39842202	2NST
1553-1	DA502E	88800100	3SYT
1553-2	DA502F	88800101	3SZT
1553-3	DA502G	88800102	3TAT
1553-4	DA502H	88800103	3TBT
1553-5	DA502J	88800104	4UYT
1553-6	DA502K	88800105	4UZT

Various bit patterns are output on the 1553-X unit and input on the 1544-X unit; the digit inputs are compared with output images. Five types of bit configurations are output to the 1553-X:

1. $FFFF_{16}$ on one output; all others 0000_{16}.
2. 0000_{16} on one output; all others $FFFF_{16}$.
3. User input pattern on one output; all others 0000_{16}.
4. Left-shifting one bit on one output; all others 0000_{16}.

5. Left-shifting a zero bit on one output; all others $FFFF_{16}$.

After each output and input, checks are made for errors detected by driver routines. Any errors sensed result in the outputof diagnostic messages.

The 1553-X DOU and the 1544-X DIU must be mounted in a 1750-1 Computer Interface Unit or a 1750-2 Computer Interface Expander connected directly to a 1750-1.

OPERATING INSTRUCTIONS

Once TSTDIO is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN IOM DIGITAL I/O TEST
TESTS, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1),(Field 2) (CR)

Where Field 1 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

Bit 5 = "1" Do Test 5

The remaining bits are not used.

Field 2 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test will execute until halted by the user.

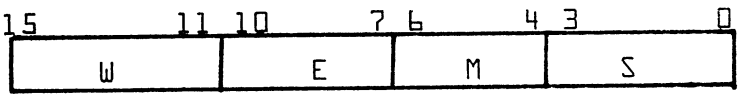
Next the user must input the test configuration information. This is requested by a message output on the SOCM as follows:

ENTER - H/W TEST CONFIGURATION INFO
1553 DIGITAL OUT 1544 DIGITAL INP
GRP - WEMS CODE,DASH NO.,WEMS CODE,DASH

Accordingly, the user must enter four control parameters on the SICM describing the hardware to be tested. This information is input in the following format:

{Field 1},{Field 2},{Field 3},{Field 4} (CR)

where Field 1 1 to 4 hexidecimal digits representing the 16 bits loaded into the 'Q' register to address the 1553-X DOU card.



where w = converter code which is normally zero

e = equipment number of the computer interface unit {1750-1}

m = module number holding the DOU

s = slot number of the DOU within the module

Field 2 1 digit representing the model number dash number of the 1553-X unit to be tested. Must be in the range of 1 to 6.

Field 3 Same as field 1 except for the 1544-X DIU card.

Field 4 Same as Field 2 except for the 1544-X DIU card, must be in the range 1 to 4.

If either fields 2 or 4 are in error, {i.e., not in the correct range} a message is output on the SOCM as follows:

TSTDIO DASH NO. ERROR

and the set of parameters is requested again.

When the set of parameters is input correctly, the operator is requested to put in the next set. The group number is output on the SOCM followed by a request for parameters. This is repeated until the operator inputs $FFFF_{16}$ for the first parameter {1553-X WEMS code} or 16 sets of parameters have been specified.

When the configuration information input is complete the test sequence execution is started.

If test three was requested, the program halts at the beginning to the first pass thru the test sequence for user input of the special test pattern as follows:

ENTER SPECIAL PATTERN FOR TEST 3

The above message is output on the SOCM and user must input one parameter on the SICM as follows:

{Field } <CR>

where Field 1 to 4 hexidecimal digits representing the special test pattern to be used in Test 3.

Upon completion of the number of repeats of the test sequence requested when halted by the user, the program outputs a message on the SOCM as follows:

END IOM DIGITAL I/O TEST, hhhh RUNS hhhh ERRORS

where hhhh is some hexidecimal number.

The program then terminates and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

Two types of error messages are output by the program; one for hardware rejects and one for discrepancies found between the image output and the image input.

Device rejects are indicated by a message in the following form:

TSTDIO TEST {1} RUN {2} {3} WEMS CODE {4} {5}

where {1} Decimal number of the test currently being executed

{2} Hexadecimal number of the current pass thru the test sequence

{3} 1553 or 1544

{4} Four digit hexadecimal address in the 'Q' register {WEMS code} where the reject occurred.

{5} INT REJ Internal reject - no response from unit

or

EXT REJ External reject - unit not ready - Most likely caused by the synchronization circuitry being enabled. Check jumper on card.

When device rejects are detected, no data compare is done.

Whenever the image input differs from the image output, the following message is output:

TSTDIO TEST {1} RUN {2} 1553 ADR {3} IS {4}
1544 ADR {5} IS {6}

where {1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} 1553 DOU WEMS code for the unit data was output to.

{4} Data output to the 1553 DOU.

{5} 1544 DIU WEMS code for the unit data was input from.

{6} Data input from the 1544 DIU.

Both types of message are output on this Standard List Device {SLD}.

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input the control parameters and the test configuration. Upon completion of these inputs each of the specified test sections is conducted in sequence.

Generally, each test section involves generating some bit configuration for output to 1553-X DOU card. A time delay of 4 milliseconds is executed if a 1544-3 or 1544-4 unit is the input unit. When the output is done, a check is made to see if any rejects occurred. An input is done to the 1544-X DIU and the data is compared to the data output. When the input is done, a check is made to see if any rejects occurred. If any rejects occurred or a data compare error was detected, an error message is output on the SLD.

The specific structure of each test is as follows:

TEST SECTION 1

All output units are zeroed. The image $FFFF_{16}$ is output to one output unit. Inputs are done from all input units and the input image compared to the output image. This procedure is repeated for all units specified.

TEST SECTION 2

All output units are set to $FFFF_{16}$. Zero is output to one output unit. Inputs are done from all input units and the input image compared to the output image. This procedure is repeated for all units specified.

TEST SECTION 3

All output units are zeroed. The special test pattern input by the user is output to one output unit as in Test Section 1.

TEST SECTION 4

All output units are zeroed. Taking each output unit in turn, a bit is left-shifted sequentially from position 0 to 15. The image is output after each shift of the bit, the inputs are done from all input units and the images compared. Each channel is again zeroed once bit 15 has been set and the output/input is accomplished. This procedure is repeated for all units specified.

All output units are set to $FFFF_{16}$, and the above procedure is repeated with a zero bit being shifted and each channel reset to $FFFF_{16}$ when it is completed.

TEST SECTION 5

This test section is identical to test Section 4 with the exception that the current image is output for each output unit after each bit shift in a sequence beginning with the channel being modified.

Current version allows exercising of 16 sets only of DOU/DIO unit combination at one time. However, various internal tables can be expanded as desired.

SUPPLEMENTAL SOFTWARE

CRMDOD	Digital Output Driver Subroutine
CRMDID	Digital Input Driver Subroutine

EXAMPLE:

Given: One 1553-1 DOU and one 1544-1 DIU plugged into slot number 00 of 1750-1 equipment number 8.

One 1553-2 DOU plugged into slot number 05 of same 1750-1 cabled to a 1544-3 plugged into slot number 14 of a 1750-2 module address 3 connected to same 1750-1.

One 1553-6 DOU plugged into slot number 10 of 1750-2 module number 07 connected to a 1750-1 with equipment number A. The 1553-6 is cabled to a 1544-4 plugged into slot number 00 of a 1750-1 equipment number C.

Test sections 1, 2, 3 and 4 will be run for 10_{16} passes.

```
(MT)
CONTROL WORD, PGM NAME
START, TSTDIO        (CR)
BEGIN IOM DIGITAL I/O TEST
TESTS, RUNS
1E, 10     (CR)
ENTER - H/W TEST CONFIGURATION INFO
        1553 DIGITAL OUTPUT   1544 DIGITAL INPUT
GRP - WEMS CODE, DASH NO., WEMS CODE, DASH NO.
#01     0400, 1, 0400, 1    (CR)
#02     0405, 2, 043E, 3    (CR)
#03     057A, 6, 0600, 4    (CR)
#04     FFFF                (CR)
ENTER SPECIAL PATTERN FOR TEST 3
5678     (CR)
TSTDIO TEST 3 RUN 0002 1553 WEMS CODE
                       0400 INT REJ
TSTDIO TEST 5 RUN 000F 1553 ADR 057A
           IS FDFF 1544 ADR 0600 IS FCFF
END IOM DIGITAL I/O TEST, 0010 RUNS 0002 ERRORS
```

PROGRAM NAME CRTPTR

MNEMONIC NAME TSTPTR

PROGRAM FUNCTION The Printer Test Routine tests the operation of the 1750-501-505 or the 1742-HRC300 Line Printer sub-systems. The operating system druver PTRDVR is used for all communications with the printer. The test routine provides tests for variable buffer, ripple pattern, clarity, hammer, spacing and 6 line/8 line per inch line density. Although the driver allows the use of format tape levels, the test does not exercise those features.

OPERATING INSTRUCTIONS Once TSTPTR is in control, a message is output on the Standard Output Comment Medium {SOCM} as follows:

```
BEGIN PRINTER TEST
TESTS/RUNS/
```

The program then enables the Standard Input Comment Medium {SICM} for user input of three control words in the following format:

{Field 1}, {Field 2} (CR)

where: Field 1 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

Bit 5 = "1" Do Test 5

Bit 6 = "1" Do Test 6

Field 2 — 1 to 4 hexadecimal digits representing the number of times the test sequence is to be run. If bit 15 is set, the test will execute until halted by the user.

Next, a message is output on the SOCM as follows:

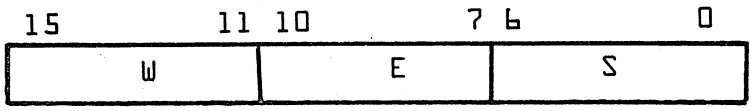
1742 INT LINE, WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

where: Field 1 — the decimal interrupt line number for the 1740 or 1742 line printer controller, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1740 or 1742 controller.



where W = converter code - which must be the value for direct data transfer if the 1740/1742 is connected via a 1706/1716. {Note: driver does not support buffered I/O}; or zero if the 1740/1742 is not connected via a 1706.

E = equipment code for the 1740/1742 controller

S = station address for director status 1.

The interrupt line input is checked for correct range and to determine if it is currently busy. If the line number is not in range or is currently busy, the following message is output on the SOCM:

TSTPTR INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

If the 1740/1742 printer is being used by CRRTMS for the Standard List Device (SLD) and the SLD is currently active printing when this test is started, then the following message is output and the test is terminated.

TSTPTR PRINTER ACTIVE

If the printer is the SLD but is not currently active, the test execution is started and all messages output to the SLD will be re-routed to the SOCM while this test is executing.

Once test execution is started, the test sections are executed in order if specified by the user. At the end of each pass through the test sequence, a pass counter is updated and compared to the number of passes requested by the user.

Upon completion of the number of repeats of the test requested, or when halted by the user, a message is output on the SOCM as follows:

END PRINTER TEST

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

Error messages output by the program are variations of one basic format as shown below:

TSTPTR TEST {1} {2} {3} {4}

where: {1} Decimal number of the test currently being executed when the error occurred.

{2} This part may or may not be output depending on the type of error. If it is output, it is one of the following:

TIME OUT No interrupt within the driver time limit.

BUFF OV External reject on data output - printer received more than 136 characters.

INT REJ Internal reject - no response from printer.

EXT REJ External reject - printer could not accept function.

{3} This part also may or may not be output. It is only output when the Alarm bit is is set in the hardware status word, then the message ALARM is output.

{4} This part is always output and is either CNTRL NOT READY or CNTRL READY depending on the Ready bit in the hardware status word.

Two examples of these error messages are shown below:

```
TSTPTR TEST 1 CNTRL NOT READY
TSTPTR TEST 1 EXT REJ ALARM CNTRL NOT READY
```

The error messages are output on the SOCM.

PROGRAM DESCRIPTION

Before the test sequence is conducted, the user must specify the particular tests to be executed, the number of runs to be made, the interrupt line and WES code for the 1740/50X-1742 line printer.

The program offers six different tests:

TEST SECTION 1 - VARIABLE BUFFER TEST

A Page Eject is executed and a complete line of 136 characters composed of the allowable character set {64} in drum order is output. The character set is decreased by 8 characters and output again. This procedure is repeated until only 8 characters are output; the string is then repeatedly increased by 8 and output until it is again 136 characters in length.

TEST SECTION 2 - RIPPLE PATTERN TEST

A Page Eject is executed and a complete line of 136 characters composed of the allowable character set {64} in drum order is output. The character set is left-shifted one position and again output. This procedure is repeated until the character set has been shifted and output 136 times.

TEST SECTION 3 - CLARITY TEST

A Page Eject is executed and a line of hammer numbers is printed followed by two line feeds. One complete line of each of the allowable characters is then output.

TEST SECTION 4 - HAMMER TEST

A Page Eject is executed and a line of hammer numbers is printed followed by two line feeds. A complete line of even hammers is printed using the character "A" (i.e., each even-numbered hammer prints an A). A complete line of odd hammers is printed using the character "B". This procedure is repeated 20 times.

TEST SECTION 5 - SPACING TEST

A Page Eject is executed and then 8 lines of Single Space printing are output by direct command to the printer (i.e., via the Escape Code) with the message SINGLE SPACE. Then 8 lines of Double Space printing are output to the printer by direct command to the printer with the message DOUBLE SPACE. During this test, the request code for output is changed from Formatted to Non-formatted.

TEST SECTION 6 - 6 LINE/8 LINE,LINE DENSITY TEST

A Page Eject is executed and then 24 lines of 6 lines per inch line density are output with the message 6 LINES/INCH. Then by direct code to the printer, the printer is changed from 6 to 8 lines per inch. Twenty-four lines of 8 lines per inch line density are output with the message 8 LINES/INCH. After the last line, the printer controller is cleared by direct command via the escape code. This returns the printer to 6 lines per inch.

SUPPLEMENTAL SOFTWARE

PDTPTR Physical Device Table for PTRDVR Driver
PTRDVR MSOS 3.0 QSS Driver for 1740/1742 Line Printer

EXAMPLE:

```
MI
CONTROL WORD, PGM NAME
LOAD, TSTPTR    CR
BEGIN PRINTER TEST
TESTS, RUNS
7E, 5   CR
1742 INT LINE, WES CODE
4, 201    CR
END PRINTER TEST
MI
CONTROL WORD, PGM NAME
START, TSTPTR    CR
BEGIN PRINTER TEST
TESTS, RUNS
7E, 1    CR
1742 INT LINE, WES CODE
4, 201    CR
TSTPTR TEST 1 EXT REJ ALARM CNTRL NOT READY
TSTPTR TEST 1 CNTRL NOT READY
TSTPTR TEST 1 CNTRL NOT READY
END PRINTER TEST
```

PROGRAM NAME CRTSIO

TEST MNEMONIC TSTSIO

PROGRAM FUNCTION

This routine tests the performance of the 1595-X Serial Input/Output Card (SIO). The cross reference between product number, EC and card type are as follows:

1595-10*	DK605A	2NXT	39917400
1595-11	DK605A	2NXT	39917400
1595-20*	DK605B	2NYT	39918200
1595-21	DK605B	2NYT	39918200

*also includes a power supply.

Operation of the test requires that the output of the 1595 under test be jumpered to the input of the same board.

The test is divided into two main test sections:

1. Interface Test
2. Data Input/Output Test

All possible error conditions are monitored and and a message output for each error condition detected.

The 1595-X SIO must be mounted in a 1750-1 Computer Interface Unit or a 1750-2 Computer Interface Expander connected directly to a 1750-1.

OPERATING INSTRUCTIONS

One TSTSIO is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

BEGIN 1595-X SIO CARD TEST
TESTS, RUNS

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

where: Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

The remaining bits are not used.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test will execute until halted by the user.

Next, a message is output on the SOCM as follows:

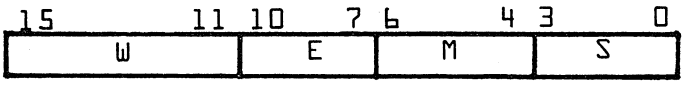
1595-X INT LINE, WEMS CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

where: Field 1 — the decimal interrupt line number for the 1595-X card, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1595-X {SIO}.



where W = converter code which is normally zero.

E = equipment number of the computer interface unit.

M = module number holding the STU

S = slot number of the STU within the module.

The interrupt line input is checked for correct range and if currently busy. If the line is busy but assigned to a system timer, busy condition is excepted. If the line number is not in range or is illegally busy the following message is output on the SICM:

TSTSIO INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

Following correct input of the interrupt line number, a message is output on the SOCM as follows:

BAUD RATE, EOT CHAR

Accordingly, the user must enter two parameters in the following format:

{Field 1}, {Field 2} (CR)

where:

Field 1	1 to 4 decimal digits representing the selected baud rate of the 1595 SIO card. Must be one of the following 75, 150, 300, 600, 1200, 2400, 4800 or 9600.
Field 2	1 to 4 hexadecimal digits representing the EOT character selected on the EOT selector switches on the STO card. If equal to $FFFF, the selector switches are all in the neutral position and no EOT interrupt will be received.

Upon completion of the number of repeats of the test sequence requested or when halted by the user, the program outputs a message on the SOCM as follows:

END 1595-X SIO TEST, hhhh RUNS hhhh ERRORS

where hhhh is some hexadecimal number.

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

When error conditions are detected, a message is output to describe the error condition. All error messages are preceded by a message segment as follows:

TSTSTU TEST d RUN hhhh

where d is the test section currently executing.

hhhh is the current pass through the test sequence

This message segment is followed by one of the following message segments to complete the description of the error detected.

aaa REJECT Q = hhhh A = hhhh X = hhhh

where aaa is EXT OR INT for the type of reject detected

hhhh is a hexadecimal number

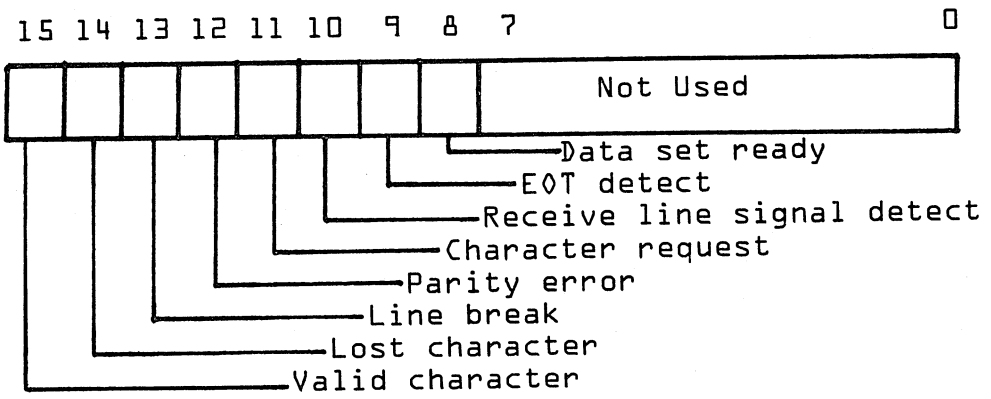
This message means that an external or internal reject has occurred with the Q, A and X register contents as specified by the hexadecimal digits.

STATUS ERROR, ACTUAL hhhh EXPECTED hhhh

where hhhh is a hexadecimal number.

This message indicates that the status input is not that which was expected. The raw H/W status will not appear in the message as some status bits are irrelevant to operation under test.

The status bits are defined as follows:



aa REPLY WHEN EXT RE, EXPECTED

This message means that a reply was received on a data I/O operation when the transmitter was full {no next character status} aa = TX or when the receiver was empty {no valid character status} aa = RX.

NO aa INTERRUPT

This message indicates that the type of interrupt indicated by aa {RX or TX} was not received in the time allotted. It might well indicate that the interrupt line as entered as a control parameter was incorrect.

DATA ERROR, ACTUAL hhhh EXPECTED hhhh

where hhhh is a hexadecimal number.

This message indicates that the data received does not compare to the data output to the transmitter. No check is done on parity bit.

NO EOT INTERRUPT

This message indicates that the EOT character specified by the user did not create an EOT Interrupt after the character was received and read via a data transfer read.

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input control parameters which specify the desired test sequence, the number of times to execute the test sequence, the 1595-X interrupt line, 1595-X WEMS code, the baud rate selected on the card and the EOT character selected if any. Given these parameters, the program selects the interrupt line and proceeds to perform the test section in order if requested.

TEST SECTION 1

This test section exercises all functions and statuses of the SIO card. Checks are made for illegal rejects and replys dependent on the state of the hardware. Interrupts are enabled and checks are made that they occur with the proper status set. If an EOT character was specified a check is made for interrupt on receiving the character.

TEST SECTION 2

The SIO card is cleared and a simple check made for interrupts. The data I/O operation transferring all characters from 00 to 7F is done and timed by the baud rate specified. When this transfer is complete, the receiver status and received data is checked for each character transmitted. If the delay time expires before the data transfer is complete, the data check is by-passed to save erroneous data print outs. The current values of the word count are output instead.

At the conclusion of each pass through the test sequence specified, a pass counter is updated. When the number of passes specified is completed or when the sequence is halted by the user, the interrupt line is released and the program outputs the end message and terminates.

EXAMPLE

Given: 1595-X card plugged into 1750-2 module address 1, connected to 1750-1 equipment addresses E & F. The 1595 card occupies slot address 3. The ready flag of slot 3 is connected to terminal which is subsequently cabled to interrupt line 15 of the CPU. The 1595 card is set up for 9600 baud transmission rate and the EOT Character is 03.

```
MI
CONTROL WORD, PGM NAME
START,TSTSIO     CR
BEGIN 1595-X SIO CARD TEST
TESTS,RUNS
6,5    CR
1595-X INT LINE,WEMS CODE
15,693     CR
BAUD RATE,EOT CHAR
9600,03   CR
TSTSIO TEST 1 RUN 0004 STATUS ERROR,
ACTUAL 8000 EXPECTED 8200
TSTSIO TEST 2 RUN 0005 STATUS ERROR,
ACTUAL 9000 EXPECTED 8000
TSTSIO TEST 2 RUN 0005 DATA ERROR,
ACTUAL 0000 EXPECTED 0065
END 1595-X SIO TEST, 0005 RUNS 0003 ERRORS
```

PROGRAM NAME CRTCRD

TEST MNEMONIC TSTCRD

PROGRAM FUNCTION

The Card Reader/Punch Test Routine is a set of tests designed to exercise and determine the performance of the 1728/430 Card Reader/Punch or the 1729-2 Card Reader using the operating system driver. The following types of tests are executed:

1) Random Data Pattern

2) Alternate Pattern ($AAA, $555)

3) Read Sync Pattern

4) User Selected Pattern

OPERATING INSTRUCTIONS

Once TSTCRD is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN CARD R/D TEST
TEST, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

Where Field 1 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = '1'	Do Test 1
Bit 2 = '1'	Do Test 2
Bit 3 = '1'	Do Test 3
Bit 4 = '1'	Do Test 4
Bit 5 = '1'	Do Test 5
Bit 6 = '1'	Do Test 6

Bit 7 = '1' Do Test 7

Bit 8 = '1' Do Test 8

Bits 9 thru 14 not used

Bit 15 = '1' If test 4 or 8 is selected, punch or read columns 39 and 40

Field 2 1 to 4 hexadecimal digits representing the number of times the test selected is to be executed. If bit 15 is set, the test will execute until halted by the user.

Next, a message is output on the SOCM as follows:

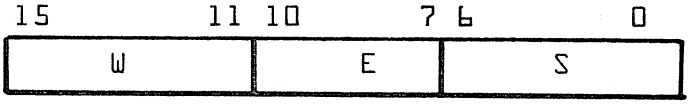
1728 INT LINE, WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

Where Field 1 the decimal interrupt line number for the 1728. Controller Common Interrupt Line must be in the range 2 to 15.

Field 2 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the '0' register to address the 1728 controller for level one status or function commands as shown below:



where W = converter code which must equal zero if the 1728/430 is not connected via a 1706; must equal code for direct transfers if the 1728/430 is connected via a 1706. {See 1700 Codes Book}

E = equipment number of the 1728 controller.

S = station address for level one status or function commands. Can equal $41, $21 or 1.

The interrupt line is checked for correct range and if currently busy. If the line number is not in range or the line is currently assigned to another unit (Busy), the following message is output on the SOCM:

TSTCRD INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

Following correct input of interrupt line number, a check is made to see if Test 3 or 7 is requested. If either test section is requested, a message is output on the SOCM as follows:

ENTER SPECIAL PATTERN FOR TEST d

where d is 3 or 7.

Accordingly, the user must enter one control parameter on the SICM in the following format:

(Field) (CR)

Where Field — 1 to 4 hexadecimal digits representing the special pattern to be used for the 60 sixteen (16) bit words punched or read from the standard ANSI data card.

If the 1728/430 is the CRRTMS loader device and the loader is busy when TSTCRD is started, the following message is output on the SOCM and the test is terminated.

TSTCRD CARD R/P ACTIVE

Upon completion of the number of repeats of the test section requested (one repeat equals one card read or punched) or when halted by the user, the program outputs a message on the SOCM as follows:

END CARD R/P TEST, hhhh RUNS, hhhh ERRORS

Where hhhh is some hexadecimal number.

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

Whenever error conditions are detected by the MSOS driver, the test routine uses a combination of the ALTDEV error code, LEVEL 1 status {word 12 of PHYSTAB}, and LEVEL 2 status input by test routine. All irregular status conditions are output. All error messages are of the same general format as follows:

TSTCRD TEST d RUN hhhh {description}

Where d is the current test section being executed

hhhh hexadecimal number of the current pass through the test section.

{description} is one of the following:

NO INTERRUPT no interrupt received by driver during specified time interval.

CKSUM ERROR check sum on formatted record was not that which is expected {check for data errors}.

INT REJ no response from 1728 controller.

EXT REJ reject received from 1728 controller. Normal followed by some other abnormal status condition.

NO 7-9 PUNCH card read without a 7-9 punch in column 1 when trying to read a formatted record.

NON-NEGATIVE RCD LENGTH word count of a formatted record was not negative.

DATA INT AFTER COL 80 data interrupt received after 80 columns processed.

EOP INT BEFORE COL 80 end of operation interrupt received before 80 columns processed.

*NOT RDY Ready status not set when expected.

BUSY Busy status set when not expected.

LOST DATA Data input attempted after data lost by the controller.

MOTION FAILURE (Feed Alert) indicates that sometime during card cycle, there was a failure in the transport of the card.

*CHIP BOX FULL Chip box full or not installed.

*HOPPER EMPTY Input hopper empty.

*STACKER FULL Output stacker full.

*FEED FAILURE failed to receive a card in the Read Ready Station after a feed command was issued and there were cards in the input hopper.

READ AREA JAM card jam in read head area.

PUNCH AREA JAM card jam in punch head area.

STACKER AREA JAM card jam in post punch station area.

PRE-READ ERROR an amplifier failure in the Read Head was detected.

PUNCH ERROR the results of the punch echo check do not agree with the requested punch information.

*MANUAL maintenance panel FEED switch is in the ON position.

*INTERLOCK interlock to mechanical area of card transport open.

*INHIBIT SW. SET punch inhibit switch set when attempting to execute punch test section.

DATA ERROR COL dd ACTUAL hhh EXPECTED hhh output when a data error is detected when comparing expected value to actual value dd = decimal column number, hhh is

a three digit hexadecimal value representing the punched data on the card starting with 11 row in the most significant bit.

If any of the errors indicated by an * is detected, execution of the diagnostic is discontinued with the following message being output.

ENTER RESUME, TSTCRD - TO CONTINUE

When the error condition is cleared, the execution can be continued by entering command as indicated. The diagnostic cannot be started (START or SETRUN) until after RESUME has been entered and the diagnostic terminates in the standard manner (ie. completion of test or via STOP command). If the test is to be stopped without further execution, the operator can enter STOP, TSTCRD and then RESUME, TSTCRD. This will terminate execution of diagnostic without further I/O operations.

PROGRAM DESCRIPTION

Only one test section can be executed at one time. The test section with the lowest number will be executed when more than one test section is selected. Each run specified equals processing of one punched card.

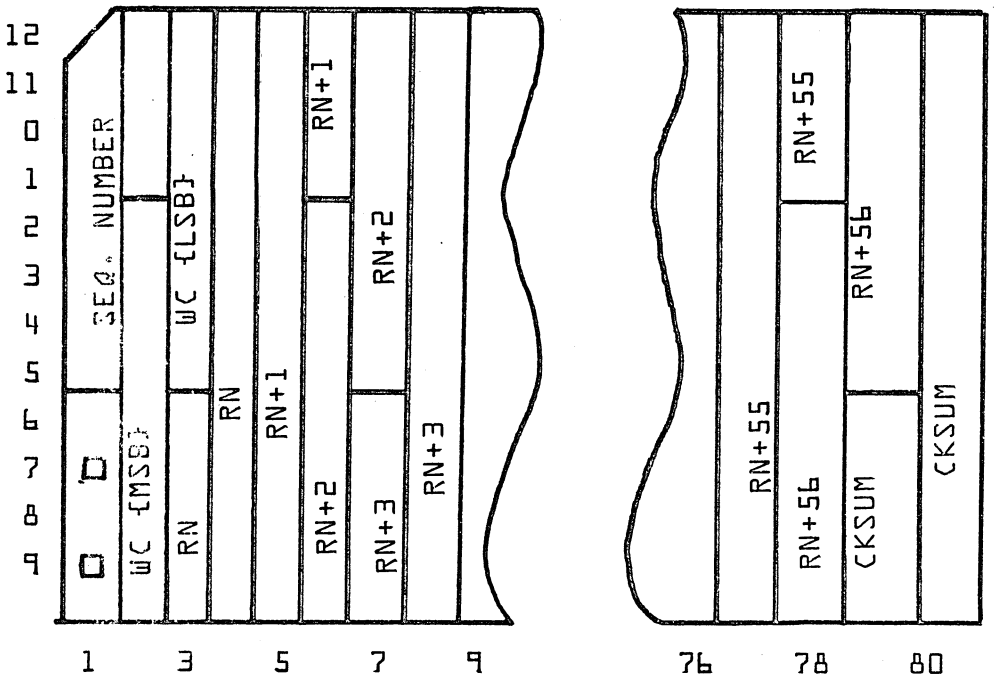
TEST SECTION 1

This section punches a standard 1700 formatted binary record. This consists of a sequence number/7-9 punch word, word count word (complemented), check sum word and 57 data words generated pseudo randomly using the following equation.

$$R_{h+1} = (R_h \times 5^5) \text{ Mod } 2^{15}$$

Where R_h = previous random number of the series

R_{h+1} = next random number of the series, Range 0-32768

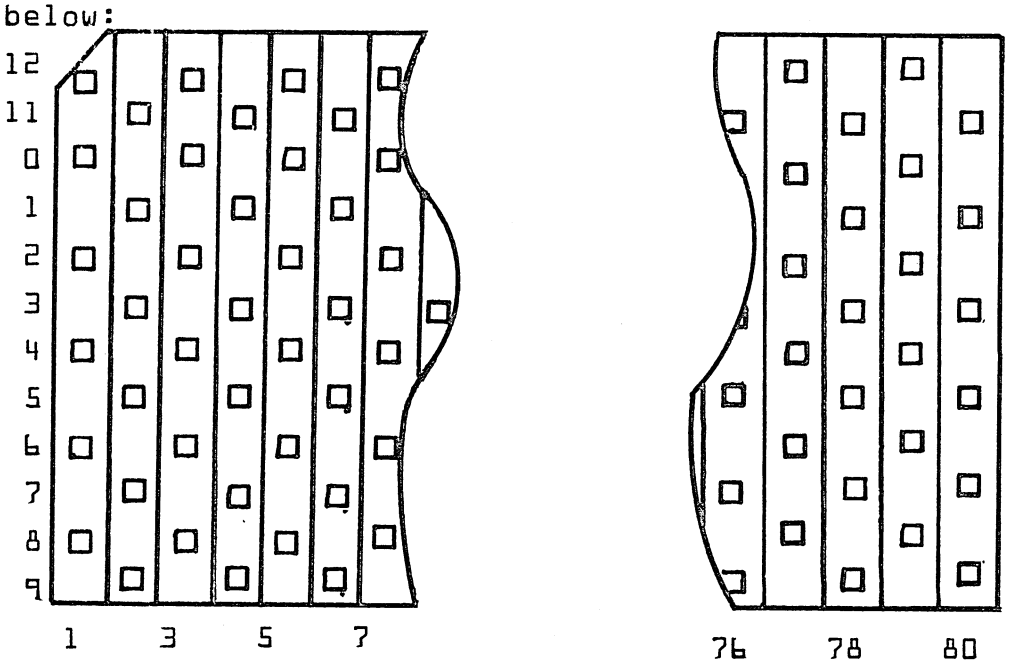


FORMATTED RECORD CARD

The random number is continued from card to card.

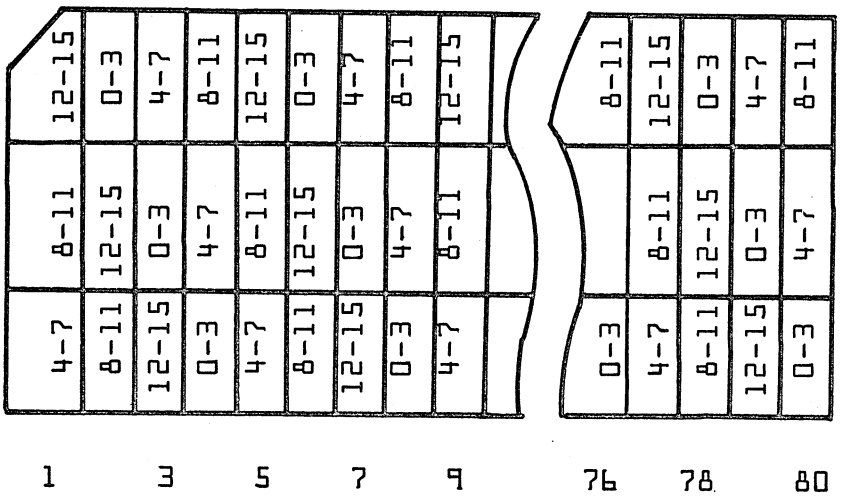
TEST SECTION 2

This section punches an alternating pattern of $AAA and $555 in a non-formatted pattern as shown below:



TEST SECTION 3

This section punches the user input pattern in 60 data words in an unformatted data card as shown below:



TEST SECTION 4

This section punches a read sync pattern of $FFF in card columns 1 and 80. If bit 15 of the TEST control parameter is set, then column 39 and 40 are also punched.

TEST SECTION 5

This section reads the pseudo random pattern, formatted record pattern punched in TEST SECTION 1. The test can only verify the data pattern for 57 data words. Any data error detected will cause on error message to be output. It is very important to maintain the sequence of the punched formatted deck.

TEST SECTION 6

This section reads the $AAA, $555 pattern punched in TEST SECTION 2. Data in all columns is verified.

TEST SECTION 7

This section reads the punched cards and compares the 60 sixteen (16) bit data words against the user specified pattern.

TEST SECTION 8

This section reads the pattern punched by TEST SECTION 4. The test should be run with the Read Sync Disable switch on the controller logic chassis in the "ON" position. The section expects all all columns on the card to be equal to zero except columns 0 and 80 which is equal to $FFF. If bit 15 of the TEST control parameter is set, columns 39 and 40 are also expected to equal $FFF.

SUPPLEMENTAL SOFTWARE

PDTCRD PHYSTAB for DR1728 Driver
DR1728 1728/430 Driver for MSOS 3.0

EXAMPLE

Given: 1728/430 with equipment number B and interrupt line //.

```
(MI)
CONTROL WORD, PGM NAME
LOAD, TSTCRD    (CR)
BEGIN CARD R/P TEST
TEST, RUNS
2, 100    (CR)
TSTCRD TEST 1 RUN 0000 EXTREJ
TSTCRD TEST 1 RUN 0000 INHIBIT SW. SET
ENTER RESUME, TSTCRD - TO CONTINUE
(MI)
CONTROL WORD, PGM NAME
RESUME, TSTCRD    (CR)
RESUME CARD R/P TEST
END CARD R/P TEST, 0100 RUNS, 0002 ERRORS
(MI)
CONTROL WORD, PGM NAME
RESUME, TSTCRD    (CR)
CONTROL WORD NOT EXPECTED
CONTROL WORD, PGM NAME
START, TSTCRD    (CR)
BEGIN CARD R/P TEST
TEST, RUNS
20, 100          (CR)
```

```
TSTCRD TEST 5 RUN 007E CKSUM ERROR
TSTCRD TEST 5 RUN 007E DATA ERROR
ACTUAL  427 EXPECTED  42F
END CARD R/P TEST, 0100 RUNS 0002 ERRORS
MI
CONTROL WORD, PGM NAME
START, TSTCRD      CR
BEGIN CARD R/P TEST
TEST, RUNS
8, 100             CR
ENTER SPECIAL PATTERN FOR TEST 3
FFFF               CR
END CARD R/P TEST, 0100 RUNS, 0000 ERRORS
```

PROGRAM NAME CRTFLX

TEST MNEMONIC TSTFLX

PROGRAM FUNCTION

The 1581/1582 Flexowriter Typewriter and Interface Test Routine tests the performance of the typewriter and interface. Specifically, the routine tests whether or not the typewriter correctly outputs and inputs all allowable characters in response to commands from the driver routine. The test routine also checks for proper operation of the color shift feature.

OPERATING INSTRUCTIONS

Once TSTFLX is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN FLEXOWRITER TEST
TEST, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

where: Field 1 — 1 to 4 hexadecimal digits representing 16-bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

The remaining bits are not used.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the selected test is to be executed. If bit 15 is set, the test is executed until halted by the user.

Next, a message is output on the SOCM as follows:

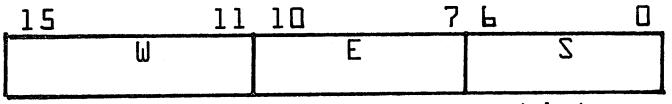
```
1581 INT LINE, WES CODE
```

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

Where Field 1 — the decimal interrupt line number for the 1581 flexowriter controller, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16-bits that are loaded into the 'Q' register to address the 1581 controller for function commands or status input.



where W = converter code which must always be zero.

E = equipment number of the 1750 Data and Control Terminal {DCT}

S = Station Address on the 1750 DCT Data and Control Buss {DCB}.

The interrupt line input is checked for correct range and if currently busy. If the line is not in range or is currently busy, the following message is output on the SOCM:

TSTFLX INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

Following correct input of the interrupt line number, a message is output on SOCM if Test 1 was requested as follows:

CHARS/LINE

Accordingly, the user must enter the number of characters per line in the following format:

{Field} (CR)

where Field — the decimal number of characters to be output per line. Range of number 1 to 258.

Following input of the line length {if required} execution is started on the test section requested. After each pass through the test section requested, a pass counter is updated and compared against the number of passes requested, if equal, the test is terminated and the following message is output on the SOCM:

END FLEXOWRITER TEST

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

At the return from each I/O request, a check is made for driver detected errors. If an error condition is detected, one of the following messages is output on the Standard List Device {SLD}.

TSTFLX TIME OUT	No interrupt received during driver time limit
TSTFLX ALARM*	Typer failed to case shift. Typer failed to cycle. Typer failed to turn power on.
TSTFLX PARITY	Bad character parity on input.
TSTFLX INT REJ	Internal reject, no response from typer interface.
TSTFLX EXT REJ*	External reject, typer controller not ready - typer hung in a cycle or typer not cabled to controller

*These messages are followed by the message:

H/W STATUS = hhhh

where hhhh is the last available controller status.

PROGRAM DESCRIPTION

The test structure for each test is as follows:

TEST SECTION 1

This section outputs the allowable character set, both upper and lower case alpha characters, repeated until the specified number of characters is reached. The line is first output in red ribbon then in black. This is repeated the number of times specified.

TEST SECTION 2

The section outputs the message INPUT CHARACTER STRING in red ribbon. The user should input a string of allowable characters followed by a carriage return {RETURN}. The number of characters input is limited to 256. The driver is monitored by the diagnostic clock, therefore, the user must input a character every minute to avoid a Time Out condition. If a Time Out occurs, the current contents of the buffer are output. When the user inputs a carriage return, the test outputs the data received from the typewriter. Then the test returns for input.

TEST SECTION 3

The test requests input as in Test 2 but the data is output continuously the number of times requested.

On input, all lower case alpha characters are converted to upper case. "Beta" character is interpreted as RUB OUT.

SUPPLEMENTAL SOFTWARE

PDTFLX - FLXDVR - Physical Device Table
FLXDVR - Flexowriter Driver {MSOS 4.0}

EXAMPLE:

Given: 1581 Flexowriter Controller with a station address of #31 on the DCB from a 1750 DCT with equipment code of 8. 1581 interrupt line is 6.

```
(MI)
CONTROL WORD, PGM NAME
LOAD, TSTFLX    (CR)
BEGIN FLEXOWRITER TEST
TEST, RUNS
2, 5     (CR)
1581 INT LINE, WES CODE
6, 431   (CR)
CHARS/LINE
258      (CR)
END FLEXOWRITER TEST
(MI)
CONTROL WORD, PGM NAME
SETRUN, TSTFLX    (CR)
BEGIN FLEXOWRITER TEST
TSTFLX ALARM H/W STATUS = 8002
TSTFLX ALARM H/W STATUS = 8002
END FLEXOWRITER TEST
```

PROGRAM NAME CRTLSC

TEST MNEMONIC TSTLSC

PROGRAM FUNCTION

This routine tests the performance of the 1573 Line Synchronizing Clock (LSC). The test routine enables and disables the interrupts and sync pulses from the clock, counts the interrupts from the clock under user control. If the LSC is also the System Timer (See Section 2) the test routine makes TIMER requests to demonstrate the long term stability of the clock.

OPERATING INSTRUCTIONS

Once TSTLSC is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN 1573 LSC TEST
TESTS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of one control parameter in the following format:

(Field) (CR)

Where Field — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1
Bit 2 = "1" Do Test 2
Bit 3 = "1" Do Test 3
Bit 4 = "1" Do Test 4

The remaining bits are not used.

Next, a message is output on the SOCM as follows:

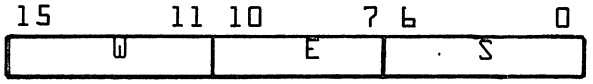
```
1573 INT LINE, WES CODE
```

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

Where: Field 1 — The decimal interrupt line number for the 1573 LSC must be in the range 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits loaded into the 'Q' register to address the LSC.



where: W = Converter code which must be zero.

E = Equipment number of the 1750 DCT.

S = Station address of 1750 DCT, must be zero.

The interrupt line input is checked for correct range and if currently busy. If the line is busy but assigned to the System Timer, the busy condition is accepted. If the line number is not in range or is illegally busy, the following message is output on the SICM:

TSTLSC INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again; if this error is repeated three times in succession, the test is terminated.

PROGRAM DESCRIPTION

Following correct input of the interrupt line number, test execution is started. Test sections 1, 2 and 3 required user parameter input.

TEST SECTION 1 -

When Test Section 1 is requested, the following message will be output on the SOCM:

ENABLE/DISABLE TEST
ENTER # OF RUNS

Accordingly, the user must enter one control parameter on the SICM in the following format:

{Field} (CR)

Where: Field — 1 to 4 hexadecimal digits representing the number of times this test section is to be executed. If bit 15 is set, the test section will execute until halted by the user.

The test then begins to execute. All possible combinations of function codes are output to the LSC via the 1750 DCT function word. Checks are made to see that interrupts are received when expected and not received when not expected. All error conditions detected are described in error messages. The sync signals are enabled and the user must use a scope to verify that these occur. This stest will use all available time at priority level 4 which will not allow other tests to run.

TEST SECTION 2 -

When test section is requested, the following message will be output on the SOCM:

INTERRUPT COUNT TEST

This message will be followed by a message and request for user input as follows:

IPS = {Field} (CR)

The user must enter the decimal value of the number of interrupts expected during a one second time period. This value should correspond with the jumper position on the Gray Counter Card {1750 DCT card position 33} and the power line frequency. The table that follows shows the typical values for 50 and 60Hz.

	50Hz	60Hz
X1	50	50
X2	100	120
X4	200	240
X8	400	480
X16	800	960
X32	1600	1920
X64	3200	3840
X128	6400	7680

The test routine then uses the CPU cycle time to execute a timing loop which is corrected for the number of expected interrupts. If the received value is within ±5% of the expected value then the expected value is assumed. The test user is notified of the results of the timing test by a message output on the SOCM as follows:

IPS = dddd

Where dddd is a four digit decimal number indicating the number of interrupts received. If the received value was within ±5% of the expected value, the expected value is output, otherwise, the received value is output.

The user is again requested to input the number of IPS. The user can run the test section again by inputting a decimal value, or $FFFF can be entered which will signal that the test section is to be terminated.

TEST SECTION 3

This test section requires that the LSC be the System Timer. This means that at monitor loading time, the System Timer was declared to be a 1573 LSC. If this was not done, then this section will not execute. If the LSC is the System Timer, then a message will be output on the SOCM as follows:

```
TIMER REQUEST TEST
MINS,REPTS
```

Accordingly, the user must input two control parameters on the SICM in the following forma.

{Field 1},{Field 2} (CR)

Where	Field 1	1 or 2 hexadecimal characters indicated the number of minutes between message outputs on SOCM indicating time since start of test section. Must be in the range of 1 to $5A_{16}$ {1 to 90_{10}}.
	Field 2	1 to 4 hexadecimal digits indicated the number of times the message is to be output.

The test performs a system timer request for the length of time specified. The request is made in tenths of a second rather than minutes to allow for greater precision. This then causes the maximum length of time between messages to be 90_{10} minutes. If the user wishes to verify the time via a stop watch; this should be done by starting the stop watch at the start of printing of one message to the start of printing of the next message. No other test routines should be outputting messages simultaneously. The timing messages are output on the SOCM in the following format:

```
TSTLSC dddd MINS SINCE START TEST 3
```

where: dddd is the decimal number of minutes since start of Test 3. After 9999_{10} the value of dddd is meaningless.

The test section may be stopped via the STOP, TSTLSC command but the current time delay must complete before the test will terminate.

TEST SECTION 4

This test section also requires the System Timer. The test enables the SYNC output to allow the user to scope the sync pulse for correct shape and interval. A message is output on the SOCM to notify the user that this condition is set.

```
SYNC ENABLED
SCOPE TO CHECK
```

A one minute time delay is then executed followed by termination of the test sequence.

When the test sequence is complete or halted by the user a message is output on the SOCM as follows:

```
END 1573 LSC TEST, hhhh ERRORS
```

Where hhhh is some hexadecimal number.

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

When error conditions are detected, messages are output on the SOCM indicating type of error. These error messages are described below:

```
TSTLSC NO TIMER
```

Before the test sequence is started, the status of the 1750 DCT is checked for bit 6, "1573 PRESENT", and if it is not set, the above message is output:

```
TSTLSC TEST d -
aaa REJECT Q = hhhh  A = hhh  X = hhhh
```

where

aaa	INT for internal reject indicating no response from the 1750 DCT EXT for external reject indicating the 1750 DCT set a reject signal
d	is the decimal test section currently executing.
hhhh	is a hexadecimal number.

This message is output whenever rejects are detected during I/O operations. The contents of the Q,A,X registers are output to describe the I/O operation.

TSTLSC INTERRUPT NOT ENABLED

This message indicates that no interrupt was received when expected during a 50 millisecond delay following an enable interrupt function.

TSTLSC INTERRUPT NOT DISABLED

This message indicates that an interrupt was received after a disable interrupt function was output.

TSTLSC INTERRUPT SET BY SYNC FUNCTION

This message indicates that an interrupt was received following output of a function to enable or disable sync pulse which did not include the interrupt enable function.

TSTLSC 1573 NOT SYSTEM TIMER

This message is output when either test 3 or 4 is requested and the system timer type is not a 1573.

EXAMPLE

Given: 1573 with 1750 DCT which has equipment number 8 and the 1573 is connected to interrupt line 2. Power line frequency is 60Hz.

```
MI
CONTROL WORD, PGM NAME
START,TSTLSC    CR
NOT IN CORE
CONTROL WORD, PGM NAME
LOAD, TSTLSC    CR
BEGIN 1573 LSC TEST
TESTS
1E    CR
ENABLE/DISABLE TEST
ENTER # OF RUNS
10    CR
TSTLSC TEST 1 EXT REJECT  Q = 0400  A = 1000  X = 0302
TSTLSC INTERRUPT NOT ENABLED
INTERRUPT COUNT TEST
IPS = 60   CR
IPS = 0060
IPS = 60   CR
IPS = 0060
IPS = 960  CR
IPS = 0910
IPS = FFFF CR
TIMER REQUEST TEST
MINS, REPTS
5, 3       CR
TSTLSC 0005 MINS SINCE START TEST 3
TSTLSC 0010 MINS SINCE START TEST 3
TSTLSC 0015 MINS SINCE START TEST 3
SYNC ENABLED
SCOPE TO CHECK
END 1573 LSC TEST, 0002 ERRORS
```

PROGRAM NAME CRTDA1

MNEMONIC NAME TSTDA1

PROGRAM FUNCTION

This test routine tests the performance of a 1560 Analog Output Unit (DAC) when connected to a 1534A Analog Input Subsystem (ADC - amplifier gain of 100*, 12 bit A/D converter) via a special cable, P/N
This test routine tests only current mode DAC units connected to current mode analog inputs. The test routine requires that a special load resistor be put on each DAC printed circuit board for the resistor R1.

This test routine is only to test the performance of the 1556 DAC and not the 1534A ADC. The 1534A performance should first be verified by running the test routine TSTAD1.

The test checks the DAC in two ways: one switching the DAC from zero to full scale and back again; one switching the DAC a step (count) at a time from zero to full scale and back to zero. The correct output value is verified after each DAC output.

Both the 1560 and the 1534A are checked for hardware errors after each input or output operation. All I/O operations are done via the operating system drivers for these units.

OPERATING INSTRUCTIONS

Once TSTAD1 is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN DAC NO. 1 TEST
TEST, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

*or multi-gain amplifier with gain code 02=100

Where: Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = '1' Do Test 1

Bit 2 = '1' Do Test 2

The remaining bits are not used.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the selected test is to be executed. If bit 15 is set, the test executes until halted by the user.

Next, a message is output on the SOCM as follows:

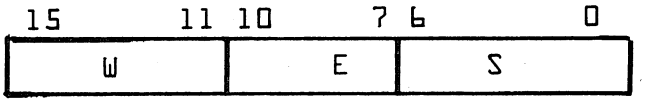
1558 INT LINE, WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

Where Field 1 — The decimal interrupt line number for the 1558 Latching Relay DAC controller, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1558 controller.



where W = converter code which must equal zero.

E = equipment number of the 1750 DCT to which the 1558 controller is cabled via the DCB.

S = DCB station address of the 1558 controller.

Next, a message is output on the SOCM as follows:

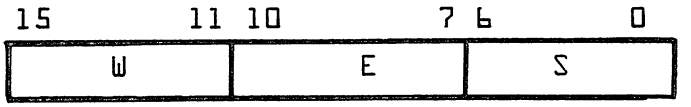
1534 INT LINE, WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

Where Field 1 — the decimal interrupt line number for the 1534 analog input controller, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1534 controller.



where: W = converter code which must equal zero.

E = equipment number of the 1750 DCT to which the 1534 controller is cabled via the DCB

S = DCB station address of the 1534 controller.

Both interrupt lines input are checked for correct range and if currently busy. If either interrupt line is busy or not correct range, a message is output on the SOCM as follows:

TSTDA1 INTERRUPT ASSIGNMENT ERROR

The set of control parameters is then requested again, if this error is repeated three times in succession, the test is terminated.

Next, a message is output on the SOCM as follows:

DAC CHNL, ADC CHNL, ALLOWABLE ERROR

Accordingly, the user must input on the SICM the channel connection information and the error criteria. Each channel set is input separately as shown below:

```
{Field 1}, {Field 2},{Field 3}    CR
{Field 1}, {Field 2},{Field 3}    CR
   |          |          |          |
   |          |          |          |
   |          |          |          |
{Field 1}, {Field 2},{Field 3}    CR
FFFF    CR
```

Where: Field 1 — 0 to 2 hexadecimal digits representing an allowable 1560 channel address.

Field 2 — 0 to 2 hexadecimal digits representing an allowable 1534A channel address.

Field 3 — 0 to 4 hexadecimal digits representing the allowable count deviation between the digital value output to the 1560 and the digital value input from the 1534A.

FFFF — Input for Field 1 when the user has specified all channel combinations to be tested. A maximum of 16 combinations can be tested at one time.

Following completion of the specification of channel connection information, a message is output on the SOCM as follows:

```
TEST x DELAY IN INCRE. OF 100ms.
```

Where x = 1 or 2

The user must enter one control parameter on the SICM as follows:

```
{Field}    CR
```

Where Field — the decimal number of increments of the 100 millisecond delay between the output of the 1560 DAC value and the input of the 1534 ADC value. Must be in range 1 to 9999.

This delay is accomplished by executing a calibrated delay loop using the CPU cycle time.

Upon completion of the number of repeats of the test requested or when halted by the user, the program output a message on the SOCM as follows:

END DAC NO. 1 TEST, hhhh RUNS, hhhh ERRORS

where hhhh is some hexadecimal number.

ERROR MESSAGE DESCRIPTION

Two types of error messages are output by the program: One for hardware errors and one for data errors outside the error criteria.

Device errors are indicated by a message in the following format:

TSTDA1 RUN {1} {2} CHNL {3} {4}

where: {1} Hexadecimal number of the current pass through the test required.

{2} Either DAC or ADC.

{3} Four-digita hexadecimal channel address.

{4} One of the following messages:

For the 1560 DAC:

INT REJ Internal reject - no response from the unit. Also could be caused by a reject from the associated 1750 Data and Control Terminal.

EXT REJ External reject-unit not ready. Caused by 1558 controller busy {not ready} or 1750 Protect Switch in reject position.

For the 1534A ADC:

INT/EXT REJ Interal or external reject from the 1534A controller, the analog channel or the associated 1750 DCT.

UNDER RANGE Analog Input channel input is under the range of the A/D converter.

OVER RANGE Analog Input channel input is over the range of the A/D converter.

When device errors are detected, no data compare is done.

Whenever the digital value input from the ADC differs by more than the error criteria for that channel set, from the digital value output to the DAC, the follow message is output:

```
TSTDA1 RUN {1} DAC CHNL {2} IS {3}
                        ADC CHNL ERROR IS {4} {5}
```

where:

{1} Hexadecimal number of the current pass through the test requested.

{2} Four-digit hexadecimal 1560 channel address.

{3} Four-digit hexadecimal value output to the 1560 DAC.

{4} Sign of the error value.

{5} Absolutized difference calculated from subtracting the DAC value output from the compensated value input from the ADC.

Both types of error messages are output on the Standard List Device {SLD}.

PROGRAM DESCRIPTION

Before the 1560 Current Mode Analog Output Unit {DAC} can be tested, it must be cabled to an equivalent type of 1534 channel {i.e. signal conditioner}. This requires that a load compensating resistor must be placed on the DAC printed circuit board in the place of resistor R1. The Table on the next page shows the configuration for each type of DAC unit. The DAC unit is cabled to the 1533/1535 Analog Multiplexer via a special test cable, Part No.

After the user inputs all test configuration parameters, the program halts for user input of the time delay between the output to the DAC and the input from the ADC in increments of 100 milliseconds.

CURRENT RANGE	1560 DAC MODEL NO.	DAC LOAD RESISTOR (R1)	1563 ① MODEL NO.
1-5 ma	1560A-D	8100 ohms	1563F
2-10 ma	1560A-D	4200 ohms	1563E
4-20 ma	1560E-H	1800 ohms	1563G
10-50 ma	1560J-M	550 ohms	1563H

Each data word output to the DAC is first left shifted five bits. After the time delay expires, the corresponding 1534A channel (1533/1535) is read. The data input is first right shifted four bits for sign extension. The resultant value is then multipled by 4 and divided by 5. This ratio of 4 to 5 comes from the fact that a 1560 current mode DAC has a range of $3FF ($1024_{10}$) counts. The 1534A current mode analog channel has a range of $43F ($1280_{10}$) counts, therefore the analog input must be compensated for this difference. The result of compensation is rounded off. After compensation, the unshifted value output to the DAC is subtracted from the compensated value. The result is adjusted by the error criteria to see if it is within the allowable error range. If not, the sign of the error is determined and the error value absolutized. An error message is then output to inform the user. If more than one DAC is being tested, all outputs are done first, then the time delay is executed and all inputs and data comparing is done.

TEST SECTION 1

Each 1560 DAC is first set to full scale. The time delay specified by the user is executed (the TC of the filter is about 35 seconds). Each 1534A ADC channel is then read and a data compare is done. Each DAC is then set to zero. The time delay is again executed followed by reading each ADC channel. Data is then compared. This constitutes one pass of the test section. If Test Section 2 is requested, this section is not executed.

---

① The 1563 Analog Signal Conditioner contains the attenuator netowrk for converting from milliamps to milli-volts. Minimum current value is converted 8 milli-volts. The maximum current value is converted to 40 milli-volts.

TEST SECTION 2

The 1556 DAC is stepped by one count increments from zero to full scale and back to zero. After each step and time delay specified by the user, executed by the system timer, the corresponding ADC channel is read and the data compared. This constitutes one pass of the test.

Every output and input is checked for device errors and if they are detected, a message is output and the data compare is by-passed.

SUPPLEMENTAL SOFTWARE

ADCDVR	1534 Analog Input Driver
PDTAD1	PHYSTAB for ADCDVR
CRMLRD	1558/1560 Driver
PDTRL1	PHYSTAB for CRMLRD

EXAMPLE

Given: 1560 DAC channels 080 to 083 cabled to 1558 controller with station address of 448 and interrupt line 9. 1533 channels 800 to 803 cables to 1534 controller with station address 456 and interrupt line 8.

```
MI
CONTROL WORD, PGM NAME
LOAD, TSTDA1    CR
BEGIN DAC NO. 1 TEST
TEST, RUNS
2, 10    CR
1558 INT LINE, WES CODE
9, 448    CR
1534 INT LINE, WES CODE
8, 456    CR
DAC CHNL, ADC CHNL, ALLOWABLE ERROR
80, 800, 6    CR
81, 801, 6
82, 802, 6
83, 803, 6
FFFF          CR
TEST 1 DELAY IN INCRE. OF 100 ms.
300    CR
TSTDA1 RUN 0001 DAC CHNL 0080 EXT REJ
END DAC NO. 1 TEST, 0010 RUNS, 0001 ERRORS
MI
CONTROL WORD, PGM NAME
SET RUN, TSTDA1    CR
BEGIN DAC NO. 1 TEST
TSTDA1 RUN 000A DAC CHNL 0083 IS 00BE
       ADC CHNL ERROR IS + 0007
END DAC NO. 1 TEST, 0010 RUNS, 0001 ERRORS
```

PROGRAM NAME — CRTHCS

TEST MNEMONIC — TSTHCS

PROGRAM FUNCTION — This routine tests the performance of the Hospital Communications System Multiplexer (HCS), DH704A/B, DH705 A-G and the channel adapter cards for both synchronous and asynchronous transmission. The test requires both transmitter and receiver cards of each type to be tested. Transmitter channels are cabled to receiver channels via cable P/N

The test is divided into three sections as follows:

1. Mux interface, interrupt and clock test

2. Force channel errors test

3. Data Transfer, Data Check Test

OPERATING INSTRUCTIONS — Once TSTHCS is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN HCS MUX TEST
TESTS, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

where Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

The remaining bits are not used.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test will execute until halted by the user.

Next, a message is output on the SOCM as follows:

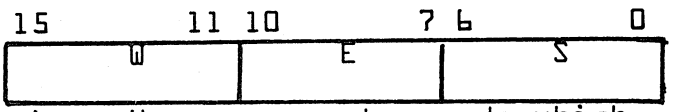
HCS INT LINE, WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

(Field 1), (Field 2) (CR)

where Field 1 — the decimal interrupt line number for the HCS Mux, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the HCS Mux.



where W = connector code which must always be zero

E = equipment number of the HCS Mux.

S = station address which must be zero.

NOTE: the HCS has equipment number softwired as $A (i.e. WES=0500) when manufactured.

The interrupt line input, is checked for correct range and if currently busy. If the interrupt line is not in range, or is currently busy, the following message is output on the SOCM:

TSTHCS INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if the error is repeated three times in succession, the test is terminated.

Following correct input of the interrupt line number and equipment address, a message is output on the SOCM as follows:

INTERRUPT INTERVAL IN MS

Accordingly, the user must enter one control parameter on the SICM as follows:

{field} (CR)

where Field — is the decimal value of the interrupt flag scan period. It must be one of the following values: 5, 10, 20, 40 or 80 milliseconds.

Next, if either test 2 or 3 was selected, the hardware test configuration is requested via the following message output on the SOCM:

```
ENTER H/W TEST CONFIGURATION INFO.
GROUP-TX CHNL, RX CHNL, TYPE, BAUD
```

Accordingly, the user must enter four control parameters for each channel set to be tested on the SOCM as follows:

{Field 1},{Field 2},{Field 3},{Field 4} (CR)

where Field 1 — 1 to 4 hexadecimal digits representing the transmit channel address. Must be in range of 0 to $7E.

Field 2 — 1 to 4 hexadecimal digits representing the receive channel address to which the transmit channel is cabled. Must be in range of 0 to $7E.

Field 3 — = 0 if transmit and receive channel are asynchronous.

= 1 if transmit and receive channels are synchronous.

Field 4 — transmit and receive channel baud rate entered as follows:

0 = 75 baud
1 = 110 baud
2 = 134.5 baud
3 = 150 baud
4 = 300 baud
5 = 600 baud
6 = 1200 baud
7 = 2000 baud
8 = 2400 baud
9 = 4800 baud
A = 9600 baud

B = 2K baud*
C = 19K baud*
D = 50K baud*
E = 256K baud*

*not available for asynchronous channels

Up to four channel sets can be tested at one time. If less than four channel sets are to be tested, test configuration input can be terminated by entering $FFFF for Field 1.

When four channel sets have been entered or the input is terminated, the execution of the test sequence is started, executing the tests in order.

Whenever a no interrupt condition is detected, the current pass through the test sequence is terminated.

At the end of each pass through the test sequence, a pass counter is updated and checked against the number of passes requested by the user. If equal or zero passes was requested, the test is terminated. The stop flag is also checked and if set, the test is terminated. The stop flag is also checked at end of each test section.

When the test terminates, the following message is output on the SOCM as follows:

END HCS TEST, hhhh RUNS, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

Each time an error condition is detected, a message is output on the Standard List Device (SLD). The error messages are of the same general format. Each message is made up of two segments. The first segment is always:

TSTHCS TEST d RUN hhhh

where d is the test section currently executing

hhhh is the current pass through the test sequence.

This first message segment is followed by one of the following error describing message sements.

aaa REJECT Q = hhhh A = hhhh X = hhhh

where aaa is EXT or INT for the type of reject detected

hhhh is a hexadecimal number

This message means that an external or internal reject has occurred with the Q, A and X register contents as specified by the hexadecimal digits.

INPUT REPLY OR EXT REJECT

This message segment is output when an attempt to do an input to the HCS controller does not cause an Internal Reject.

NO MUX INTERRUPT

This message segment is output when the mux does not interrupt at the interval rate as specified during parameter input.

MUX INT. COUNT ERROR

This message segment is output when the number of interrupts in a time period does not equal the expected amount. This message is followed by the actual and expected values.

CLOCK COUNT ERROR

This message segment is output when the value of the core clock, location $0140 is not what is expected by the program. This message is followed by the actual and expected value of the core clock.

aa CHL hhhh NO I/O ERR.

where aa = RX for receiver channels
= TX for transmit channels

hhhh = channel address

This message segment is output when a receive channel is forced to be a transmit channel or a transmit channel is forced to be a receive channel and a channel I/O error does not occur. This message is followed by the actual and expected values of the channel word count.

aa CHL hhhh WORD COUNT ERROR

where aa + hhhh are same as above

This message segment is output when at the completion of the time delay required to transfer the data buffer and the word count of the channel specified is not zero. This message is followed by the actual and expected values of the word count.

aa CHL hhhh NO INTERRUPT FLAG

where aa + hhhh are same as above

This message segment is output when at the completion of the data transfer, the interrupt flag is not set by the channel specified.

RX CHL hhhh STATUS ERR.

where hhhh is the address of the synchronous channel which the status error was detected

This message segment is output when at the completion of the synchronous channel data transfer a status error is detected. This message is followed by the actual and expected values of the synchronous channel status.

DATA ERROR RX CHL hhhh WORD wwww

where hhhh address of the receiver channel with the data error

wwww word within the buffer which is in error

This message segment is output when at the completion of a data transfer, a data compare error occurs. This message is followed by the actual and expected values of the data word.

INTERRUPT NOT DISABLED

This message segment is output when an interrupt is received from the mux controller even after a disable function is output.

PROGRAM DESCRIPTION

Before the test can be conducted, the user must enter the test parameters -- test sequence to be executed, the number of times to execute the test sequence, the HCS interrupt line number, the HCS-WES code, interrupt scan frequency and the hardware test configuration if tests 2 and/or 3 are requested.

TEST SECTION 1

This section tests the basic mux controller. The controller is tested to ensure its executing all function commands properly. The interrupt line is checked for proper interrupt frequency. The core clock is checked for proper updating and the lower 8 bits are checked for proper counting. The controller is also checked to insure that it does not accept any input commands.

TEST SECTION 2

This section checks for proper error response of the mux channel adaptor cards and mux controller by forcing errors which can be simulated. Transmit channels are set in receive mode and receive channels are set in transmit mode and a check is made for I/O errors which should be set. If the channels under test are synchronous channels, buffer overrun and CRC errors are also forced.

TEST SECTION 3

This section tests the data transfer performance of the HCS mux controller and channel adaptor cards. A data transfer is initiated on all transmit channels and their respective receiver channels. A time delay is executed, calculated as the correct time to transfer the buffers at the baud rate specified by the user. If more than one baud rate is being tested, the time delay is set for the slowest channels under

test. At the completion of the time delay, the mux controller is cleared and a check is made for proper Word Count, word contents (i.e. no I/O error and zero WC) and interrupt flag set. If synchronous channel the receiver status is also checked. Each word in the receiver buffer is checked against the expected values. If the channel is asynchronous, the upper byte of the received word is checked for proper status. All irregular conditions are reported as errors.

At the completion of each pass through the test sequence, a pass counter is updated and compared against the number of passes requested by the user. If equal or zero passes was requested, the test is terminated.

EXAMPLE

Given: HCS multiplexer with an equipment code of $A and connected to interrupt line 10. The mux has two synchronous receiver channel adaptor cards in addresses 0 and 1; two synchronous transmitter channel adapter cards in addresses 2 and 3; a 4 channel asynchronous receiver channel adapter card in addresses 4, 5, 6 and 7; and a 4 channel asynchronous transmitter channel adaptor card in addresses 8, 9, A and B. The synchronous channel adaptor cards are set for 19K baud rate. The asynchronous channel adaptor cards are set for 1200 baud rate.

```
(MI)
CONTROL WORD, PGM NAME
LOAD, TSTHCS        (CR)
BEGIN HCS TEST
TESTS, RUNS
E, 10          (CR)
HCS INT LINE, WES CODE
10,0500        (CR)
INTERRUPT INTERVAL IN MS.
5     (CR)
ENTER H/W TEST CONFIGURATION INFO.
GROUP - TX CHNL, RX CHNL, TYPE, BAUD
NO. 01  2, 0, 1, C      (CR)
NO. 02  3, 1, 1, C
NO. 03  A, 6, 0, 6
NO. 04  B, 7, 0, 6      (CR)
END HCS TEST, 0010 RUNS, 0000 ERRORS
(MI)
CONTROL WORD, PGM NAME
SET RUN, TSTHCS
BEGIN HCS TEST
```

```
TSTHCS TEST 2 RUN 0002 RX CHL 000A NO I/O ERR.
ACTUAL 0FFF EXPECTED 8000
TSTHCS TEST 3 RUN 0002 RXCHL 000A NO INTERRUPT FLAG
TSTHCS TEST 3 RUN 0002 RXCHL 000A WORD COUNT ERROR
ACTUAL 0FFF EXPECTED 0000
TSTHCS TEST 3 RUN 0002 DATA ERROR RX CHL 000A
WORD 0089 ACTUAL 0000 EXPECTED 807F
END HCS TEST, 0010 RUNS, 0004 ERRORS
```

1549 EXTERNAL INTERRUPT EXPANDER TEST ROUTINE

PROGRAM NAME CRTEXP

TEST MNEMONIC TSTEXP

PROGRAM FUNCTION

This routine tests the performance of a 1549 External Interrupt Expander Subsystem. Operation of the test requires that each 1549 station be connected to a pair of 1553, 1555 or 1558 channels via the digital I/O test box (See Appendix IV). Once all channels have been initialized, each external interrupt line (16 per unit) is tested in sequence as follows:

1. Enable all interrupt lines.
2. Disable line currently being tested, enable rest.
3. Generate interrupt on current line.
4. Check for illegal interrupt.
5. Check status of all stations.
6. Enable line currently being tested, disable rest.
7. Check for proper interrupt.
8. Check status of all stations.

After each output on 1553, 1555 or 1558, those devices are checked for any error indications returned by the driver. Each 1549 station is checked for internal or external rejects, or failure to acknowledge an interrupt. Diagnostic messages are output whenever an error is sensed.

OPERATING INSTRUCTIONS

Once TSTEXP is in control, a message is output on the Standard Output Commend Medium (SOCM) as follows:

```
BEGIN 1549 TEST
UNIT, RUNS, 1549 INT LINE
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of three control parameters in the following format:

(Field 1), (Field 2), (Field 3) (CR)

Where: Field 1 — 1 hexadecimal digit indicating the type of output unit used to generate interrupts

0 = 1553
1 = 1553/1555
2 = 1558/1559

Field 2 — 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test sequence will be executed until halted by the user.

Field 3 — the decimal interrupt line number to which the 1549 unit is connected. Must be in range of 2 to 15.

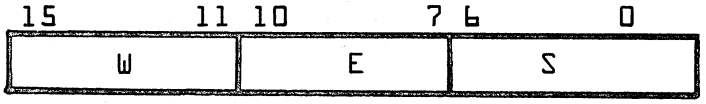
Next, a message is output on SOCM as follows:

EXP DCT WES CODE, OUTPUT DCT WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

(Field 1), (Field 2) (CR)

Where: Field 1 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1750 Data and Control Terminal (DCT) to which the 1549 External Interrupt Expander is connected.



where W = converter code which must always be zero.

E = equipment number of the 1750 DCT.

S = station address for 1750 status, always zero.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' regist to address the 1750 DCT to whi the 1553 or 1553/1555 digital output units are connected.

If the output unit specified was a 1558/1559 Latching Relay Subsystem, Field 2 above is not requested and the following message is output on the SOCM.

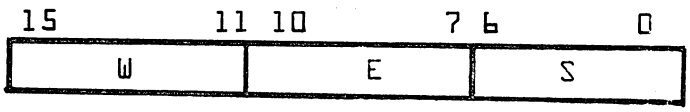
1558 INT LINE, WES CODE

Accordingly, the user must enter two control parameters on the SOCM as follows:

{Field 1}, {Field 2} (CR)

Where: Field 1 — the decimal interrupt line number for the 1558 Latching Relay Subsystem Controller must be in range 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16-bits that are loaded into the 'Q' register to address the 1558 controller.



where W = converter code which must always be zero.

E = equipment number of the 1750 DCT to which the 1558 controller is connected.

S = Data and Control Bus {DCB} station address of the 1558 controller.

Both the 1549 and 1558 interrupt lines are checked for proper range and if currently busy. If either line is not in range or is currently busy, the following message is output on the SOCM:

TSTEXP INTERRUPT ASSIGNMENT ERROR

The current line of parameters is then requested again; if this error is repeated three times in succession, the test is terminated.

Next, the message:

EXP STN, NOP CHNL, NCL CHNL

is output on the SOCM to indicate that the input is enabled on the SICM to specify what output channels are connected to each 1549 station. Thus, the user inputs:

```
jj, kk, ll      CR
jj, kk, ll      CR
.   .   .       .
.   .   .       .
.   .   .       .
FFFF            CR
```

Where:	jj	Allowable 1549 station addresses.
	kk	Normally open (NOP) output channel address.
	ll	Normally closed (NCL) output channel address.
	FFFF	Input when operator has specified all station/channel combinations used (limited to 4 or less).

On completion of the number of passes through the test sequence requested by the user, or when halted by the user, the following message is output on the SOCM:

END 1549 TEST, hhhh RUNS, hhhh ERRORS

where: hhhh is some hexadecimal digits

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

Several types of errors are output by the test routine depending on the type of failure and the type of output device used for interrupt generation.

TSTEXP RUN {1} INTR {2} {3} STN {4} STATUS {5}

Where: {1} is current pass through test sequence.

{2} is the interrupt line currently under test.

{3} type of failure detected

NO INT no interrupt received from 1549 unit

OTHER INTR interrupt bits set in status of station other than unit under test

IL INT BIT interrupt status bit set when interrupt not enabled.

NO INT BIT interrupt received but status bit expected was not received

MULT INT interrupt received with interrupt status bits set other than line under test

{4} hexadecimal station address of current unit under test

{5} hexadecimal status of the current unit under test

TSTEXP RUN{1} INTR{2} STN{3} {4}

{1}, {2} same as above

{3} hexadecimal station address of current unit under test

{4} type of failure detected

FAIL ACK interrupt status of current line under test did not reset or acknowledge command

INT REJ no response from current unit under test

EXT REJ reject sent by current unit under test

TSTEXP RUN{1} 1750 STN{2} {3}

{1} same as above

{2} 1750 WES code

{3} EXT REJ
INT REJ

TSTEXP RUN{1} {2} CHL{3} {4}

{1} same as above

{2} 1553, 1555 or 1559

{3} channel address of failing device

{4} EXT REJ
INT REJ
SELECT ERROR {1559 ONLY}

TSTEXP RUN{1} 1558 STN{2} {3}

{1} same as above

{2} 1558 WES code

{3} EXT REJ
INT REJ
TIME OUT
ALARM STATUS=hhhh
where hhhh is 1558 controller status

PROGRAM DESCRIPTION

Once the test parameters have been obtained from the user via the SICM, the program enters the initialization sequence wherein all external interrupts are disabled, normally open relays/registers are opened, normally closed relays/registers are closed, and any interrupts resulting from initialization are acknowledged. All interrupt stations are checked for status to ensure that no bits are still set. If any bits are set, a diagnostic message is output {FAIL ACK} and the test continues.

Next, the test phase is executed as follows:

All external interrupts are enabled. The external interrupt mask register is set to disable the external line currently being tested. An interrupt is generated on that line; checks are made for an illegal interrupt, and, if one was received, for failure of the 1549 to acknowledge that interrupt. In the first case, a diagnostic message is produced {IL INT} and the test continues. In the latter case, a message is output {FAIL ACK} and the test continues. The status of each 1549 station is checked for:

1. Status bits set in stations other than the current station (OTHER INTR).

2. Status bit(s) set in current station other than for current external line (MULT INT).

3. Status bit set for current external line when line has been disabled (IL INT BIT).

Next, the mask is set to enable the current line and disable the other external lines. A check is made to determine if an interrupt was received. If no interrup was received, a message isoutput (NO INT) and the test continues. The status of each 1549 station is checked for:

1. Status bits set in stations other than the current station (OTHER INTR).

2. Status bit(s) set in current station other than for current external line (MULT INT).

3. No status bit set for current line (NO INT BIT).

This procedure is repeated for each external interrupt line in each 1549 station and constitutes one run throug the test sequence. The runs through the test phase are repeated the number of times specified by the user.

Throughout the test, the occurrence of either an internal or external reject will cause a message to be output and the test continues.

SUPPLEMENTAL SOFTWARE

PDTRL1 PHYSTAB for Latching Relay Driver
CRMLRD Latching Relay Subsystem Driver
CRMDOD Logic Level Digital Output Driver

EXAMPLES

Given: 1549B External Interrupt Expander with station addresses 10, 11, 14 and 15 connected to 1750 DCT with equipment code 8. 1549 interrupt line is 10. The 1549 is cabled to a 1553 Logic Level Digital Output unit with channel addresses 000 throug 003, connected to DCT as above.

```
MI
CONTROL WORD, PGM NAME
LOAD, TSTEXP    CR
BEGIN 1549 TEST
UNIT, RUNS, 1549 INT LINE
0, 10, 10    CR
EXP DCT WES CODE, OUTPUT DCT WES CODE
400,400    CR
EXP STN, NOP CHNL, NCL CHNL
10, 0, 1    CR
11, 2, 3    CR
FFFFF    CR
END 1549 TEST, 0010 RUNS, 0000 ERRORS
```

Given: 1549 as above but cabled to 1558/1559 Latching Relay Subsystem with 1558 Station Address of $48, 1559 channel addresses $80 through $83 connected to 1750 DCT with equipment code of 9. 1558 interrupt line is 9.

```
MI
CONTROL WORD, PGM NAME
LOAD, TSTEXP    CR
BEGIN 1549 TEST
UNIT, RUNS, 1549 INT LINE
2, 10, 10    CR
EXP DCT WES CODE
400    CR
1558 INT LINE, WES CODE
9, 448 CR
EXP STN, NOP CHNL, NCL CHNL
10, 80, 81    CR
11, 82, 83    CR
FFFF    CR
END 1549 TEST, 0010 RUNS, 0000 ERRORS
MI
CONTROL WORD, PGM NAME
SET RUN, TSTEXP    CR
BEGIN 1549 TEST
TSTEXP RUN 0005 1559 CHL 0083 SELECT ERROR
TSTEXP RUN 000A INTR 0400 NO INT BIT STN 0410 STATUS 0000
END 1549 TEST, 0010 RUNS, 0002 ERRORS
```

PROGRAM NAME CRTAD3

TEST MNEMONIC TSTAD3

PROGRAM FUNCTION

This routine tests the performance of IOM 1536-2/1525-3/1501-8X Relay Analog Input Subsystem. Generally, the routine obtains inputs from a sequence of 1- to 8- channel sets, repeats a specified number of times, compares the actual to the expected counts, and generates a double-precision histogram which allows a maximum count of 9,999,999 for each error counter.

In order to conduct the test, the user must provide the expected full-scale value for each mux address being tested. This is most conveniently accomplished using the Analog Input Test Box {Control Data Part No. 39007700} ① which provides variable DC inputs to each mux address of a sequence of 8-mux address sets. With ~~the test~~ box, the user can apply the desired voltage to each of the mux addresses; then, when requested by the test routines he can enter the full scale reading {%} expected for each mux address. This information is converted by the program to expected counts {given that it has previously received correct calibration data}. The expected counts are compared to actual counts to produce a histogram of errors.

After each input, checks are made for any error indications returned by the driver. Any errors indicated result in the output of diagnostic messages.

OPERATING INSTRUCTIONS

Once TSTAD3 is in control, a message is output on the Standard Output Comment Medium {SOCM} as follows:

```
BEGIN ADC NO. 3 TEST
BEG MUX ADR, END MUX ADR, RUNS
```

The program then enables the Standard Input Comment Medium {SICM} for user keyboard input of three control parameters in the following format:

{Field 1}, {Field 2}, {Field 3} (CR)

① See Appendix

Where: Field 1 — 3 hexadecimal digits representing the lowest mux address to be tested.

Field 2 — 3 hexadecimal digits representing the highest mux address to be tested.

Field 3 — 1 to 4 hexadecimal digits representing the number of times each mux address is to be multiplexed. If bit 15 is set, the test will execute until a maximum count of 9,999,999 is recorded in any error cell or until halted by the user.

If the ending mux address input is less than the beginning mux address input, the message below is output on the SOCM and the parameters are requested again.

```
TSTAD3 ADR ERR
```

Finally, if zero runs were input or the runs field left blank no message is output but the parameters are requested again.

Next, a message is output on the SOCM as follows:

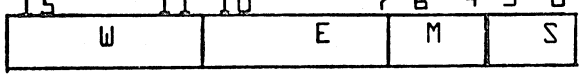
```
1536-2 INT LINE, WEMS CODE
```

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

Where: Field 1 — the decimal interrupt line number for the 1536-2 Relay Analog Multiplexer controller must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1536-2 mux controller.



where W = converter code which must always be zero.

E = equipment number of the Computer Interface Unit.

M = module address of the module holding the 1536-2 mux controller

S = slot address of the 1536-2 within the module.

The interrupt line input is checked for correct range and whether currently busy. If the line number is not in the range or is currently busy, the following message is output on the SOCM:

TSTAD3 INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

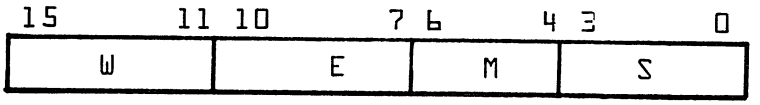
Following correct input of the interrupt line number, a message is output on the SOCM as follows:

1525-3 WEMS CODE

Accordingly, the user must enter one control parameter on the SICM in the following format:

{Field} (CR)

where: Field 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address 1525-3 ADC.



where W = converter code which must always be zero.

E = Equipment code of the Computer Interface Unit

M = module address of the module holding the 1525-3 ADC.

S = slot address of 1525-3 within the module.

Next, a message is output on the SOCM as follows:

SCALE, CK RELAY, DELAY

Accordingly, the user must enter three control parameters on the SICM in the following format:

{Field 1}, {Field 2}, {Field 3} (CR)

Where: Field 1 — 1 to 4 hexadecimal digits representing the histogram scale factor. The expected counts are subtracted from the actual counts input and the result is divided by a non-zero scale factor to product the scaled conversion error recorded in the histogram.

Field 2 — If the field is non-zero, then whenever the scaled conversion error is greater than +7 or less than -7 a message is output indicating the mux address which was out of range. {see error description page

Field 3 — 1 to 4 hexadecimal digits representing the number of 10 millisecond delays to be executed between converting each set of points.

Next, a message is output on the SOCM as follows:

% FULL SCALE, GAIN

The user must then enter eight sets of parameters to describe the expected percent full scale and gain for each mux address set. The request for each parameter set is preceeded by a message. The message and parameters request are as follows:

POINT X {Field 1} {Field 2} (CR)

Where: X — The number 1 to 8 for mux address sets 1 to 8.

Field 1 — 1 to 4 hexadecimal digits representing the expected percent full scale from the mux address set. This is a signed value {i.e. if negative the complement of the percent full is entered}.

Field 2 — 1 digit representing the amplifier gain to be used for the mux address set. The digit is a code which is defined as follows:

Code	Gain
0	1
1	10
2	100
3	1000

NOTE: Gains are typical but may vary from system to system. Always lowest gain is Code 0, highest gain is Code 3.

If the expected full scale value is unknown, the user may enter $8000 for Field 1 which signals to the test routine to use the first value input from the mux address set as the value for expected counts.

If seven or less mux addresses are requested in the first parameter request, then the mux address set information request and the histogram are abbreviated accordingly. (i.e. if 000 and 002 are input for the beginning and ending mux addresses respectively, then mux address set information is requested only for points 1, 2 and 3).

Upon completion of the number of times each mux address was requested to be multiplexed or when halted by the user, the resultant histogram is output (if the SKIP SWITCH is not set) on the Standard List Device (SLD) followed by a message on the SOCM as follows:

END ADC NO. 3 TEST, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then terminates and exits to the dispatcher.

Figure 19.1, Page 19-8 is an example of the parameter input and resultant histogram.

ERROR MESSAGE DESCRIPTION

When error conditions are detected, messages are output on the SLD to describe the error condition. These messages are of one general type as shown below:

TSTAD3 MUX ADR {1} {2}

where: {1} Four-digit hexadecimal mux address

{2} Any one of the following messages

NO 1536 INTERRUPT	no interrupt was received from the 1536-2 controller when expected.
1536 INT/EXT REJ	either an internal or external reject was received when doing an I/O instruction to the 1536-2 controller
1525-3 INT/EXT REJ	either an internal or external reject was received when doing an I/O instruction to the 1525-3 ADC.
OVER RANGE	value input from ADC for mux address stated was the maximum value that the ADC could output.
UNDER RANGE	value input from ADC for mux address stated was the minimum value that the ADC could output.
CK RELAY	Value of the scaled conversion error is outside the range of the histogram {i.e., greater than +7 or less than -7}. This message is determined by the test and is not counted as an error.

PROGRAM DESCRIPTION

The analog mux addresses are read in blocks of one to eight addresses in sequence until all addresses from the beginning address to the ending address are completed. This sequence constitutes one pass and is repeated until the number of passes equals the number specified, the user halts the test, or a histogram table cell overflows, whereupon the histogram table is generated and output along with other information.

Inputs are obtained from each mux address in the following manner. The data table used by the Analog Input Driver is filled with a sequence of mux addresses and gain designators, and the input request is executed. When control returns to the test routine each expected count is subtracted from the applicable actual counts; the result is divided by a non-zero scale factor; and a cell designated as a counter for errors of a specific magnitude on one of the eight mux address sets is incremented. If the input count is replaced with an error code, it is processed to output the appropriate diagnostic messages and ignored. The program generates the histogram by processing the tables-of-error counters.

The program allows the user to specify the full-scale voltage (%) to be applied to each channel. That voltage is converted to the equivalent expected counts. If $8000 is input for % full scale, the first data input from mux address set is stored in the counts compare table.

If the SELECTIVE SKIP key is turned on, the test routine will exit without producing the histogram.

SUPPLEMENTAL SOFTWARE

PDTAD3 Physical Device Table for D1536 Driver
D1536 MSOS 4.1 1536-2/1525-3 Driver (Deck C-23)

EXAMPLE

```
MI
CONTROL WORD, PGM NAME
LOAD, TSTAD3  CR
BEGIN ADC NO. 3 TEST
BEG MUX ADR, END MUX ADR, RUNS
0, 7, FFF  CR
1536-2 INT LINE, WEMS CODE
9, 48B  CR
1525-3 WEMS CODE
48C  CR
SCALE, CK RELAY, DELAY
1, 1, 0  CR
% FULL SCALE, GAIN
POINT 1      0, 1  CR
POINT 2
POINT 3
POINT 4
POINT 5
POINT 6
POINT 7
POINT 8      0, 1  CR

TSTAD3 HISTOGRAM OF RESULTS
SCALE FACTOR 0001 ADDR 0000-0007 RUNS 00004095
```

POINT	1	2	3	4	5	6	7	8
EX CNTS	0000	0000	0000	0000	0000	0000	0000	0000
SP/GAIN	0003	0003	0003	0003	0003	0003	0003	0003
GT	0	0	0	0	0	0	0	0
+7	0	0	0	0	0	0	0	0
+6	0	0	0	0	0	0	0	0
+5	0	0	0	0	0	0	0	0
+4	0	0	0	0	0	0	0	0
+3	0	0	0	0	0	0	0	0
+2	0	0	0	0	0	0	0	0
+1	0	0	0	0	0	0	0	0
0	4095	4095	4095	4095	4095	4095	4095	4095
-1	0	0	0	0	0	0	0	0
-2	0	0	0	0	0	0	0	0
-3	0	0	0	0	0	0	0	0
-4	0	0	0	0	0	0	0	0
-5	0	0	0	0	0	0	0	0
-6	0	0	0	0	0	0	0	0
-7	0	0	0	0	0	0	0	0
LT	0	0	0	0	0	0	0	0

```
END ADC NO. 3 TEST, 0000 ERRORS
```

PROGRAM NAME CRTREG

TEST MNEMONIC TSTREG

PROGRAM FUNCTION

This routine tests the performance of the 1553 Digital Output Interface and the 1544 Digital Input Interface. Operation of the test requires that each 1553 channel to be tested be connected to a 1544 channel. Thus, various bit patterns are output on the 1553 and input on the 1544; the digital inputs are compared with the output images. Five types of bit configurations are output to the 1553:

1. $FFFF_{16}$ on one channel; all others 0000_{16}.
2. 0000_{16} on one channel; all others $FFFF_{16}$.
3. User input pattern on one channel; all others 0000_{16}.
4. Left-shifting one bit on one channel; all others 0000_{16}.
5. Left-shifting a zero bit on one channel; all others $FFFF_{16}$.

After each output and input, checks are made for any error indications returned by the drivers. Any errors sensed result in the output of diagnostic messages.

OPERATING INSTRUCTIONS

Once TSTREG is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN 1553/1544 TEST
TESTS, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

where: Field 1 — 1 to 4 hexadecimal digits representing 16-bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

Bit 5 = "1" Do Test 5

The remaining bits are not used.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test will execute until halted by the user.

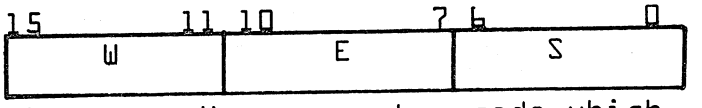
Next, a message is output on the SOCM as follows:

OUTPUT DCT WES CODE, INPUT DCT WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

where: Field 1 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1750 Data and Control Terminal {DCT} to which the 1553 Digital Output Interface is connected.

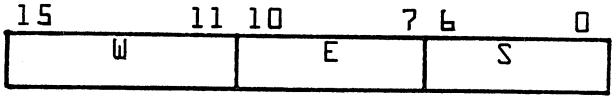


where: W = converter code which must always be zero.

E = equipment number of the 1750 DCT

S = station address of the 1750 DCT, always zero.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1750 Data and Control Terminal (DCT) to which the 1544 Digital Input Interface is connected.



where W = converter code which must always be zero.

E = equipment number of the 1750 DCT.

S = station address of the 1750 DCT, always zero.

Next, a message is output on the SOCM as follows:

OUT CHNL, IN CHNL

Accordingly, the user must input on the SICM the channel connection information. Each channel set is input separately as shown below:

(Field 1), (Field 2) (CR)

(Field 1), (Field 2) (CR)

. . .

. . .

. . .

(Field 1), (Field 2) (CR)

FFFF (CR)

Where: Field 1 — 0 to 2 hexadecimal digits representing an allowable 1553 channel address.

Field 2 — 0 to 2 hexadecimal digits representing an allowable 1544 channel address.

FFFF — Input for Field 1 when the user has specified all channel combinations to be tested. A maximum of 16 combinations can be tested at one time.

Upon completion of the number of repeats of the test sequence requested or when halted by the user, the program outputs a message on the SOCM as follows:

END 1553/1544 TEST, hhhh RUNS, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then terminates and exits to the dispatcher.

If Test 3 was requested, the test halts before beginning the test sequence for the user to input the special test pattern as follows:

ENTER SPECIAL PATTERN FOR TEST 3

The message above is output on the SOCM and the user must input one parameter as follows:

{Field 1} (CR)

Where Field 1 — 1 to 4 hexadecimal digits representing the special test pattern.

ERROR MESSAGE DESCRIPTION

Two types of error messages are output by the program: one for hardware malfunctions and one for discrepancies found between the image output and the image input.

Device reject errors are indicated by a message in the following form:

TSTREG TEST {1} RUN {2} {3} aaa {4} {5}

where:

{1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} 1553 or 1544 and aaa = CHL
1750 and aaa = STN

{4} If aaa = CHL, the four digit hexadecimal channel address

If aaa = STN, the four digit hexadecimal station address {WES CODE}.

{5} Error description

1553 or 1544

INT REJ Internal reject-no response from unit

EXT REJ External reject-unit not ready. Most likely caused by the presence of a synchronization device in the unit.

1750

INT REJ Internal reject-no response from unit.

EXT REJ External reject-unit not ready {check protect switch}.

When device errors are detected, no data compare is done.

Whenever the image input differs from the image output, the following message is output:

TSTREG TEST {1} RUN {2} OUT CHNL {3} IS {4} IN CHNL {5} IS {6}.

where: {1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} Four-digit hexadecimal 1553 channel address.

{4} Four-digit hexadecimal image output.

{5} Four-digit hexadecimal 1544 channel address.

{6} Four-digit hexadecimal image input.

Both type of error messages are output on the Standard List Device {SLD}.

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input the control words and the pair of connected channels. Upon completion of this input, each of the specified tests is conducted in sequence.

Generally, each test involves generating some bit configuration for output on a 1553 channel. When the output is accomplished; a check is made for any reject error indications returned by the driver; a digital input is accomplished on the connected 1544 channel; and a check is made for any reject error indications returned by the 1544 driver. The digital input is compared with the image output; any differences will result in a diagnostic message.

The specific structure of each test is as follows:

TEST SECTION 1

All output relays are zeroed. The image $FFFF_{16}$ is output to a channel. Digital inputs are read from all channels and the inputs are compared to the output images. This procedure is repeated for all channels specified.

TEST SECTION 2

All output relays are set to $FFFF_{16}$. A channel is zeroed. Digital inputs are read on all channels and the inputs are compared to the output images. This procedure is repeated for all channels specified.

TEST SECTION 3

All output relays are zeroed. The special pattern input by the user is output on each channel as in Test 1.

TEST SECTION 4

All output channels are zeroed. Taking each channel in turn, a bit is left-shifted sequentially from positions 0 through 15. The image is output after each shift of the bit, digital inputs are read on all channels, and the inputs are compared to the output images. Each channel is again zeroed once bit 15 has been set and output/input accomplished. This procedure is repeated for each channel specified.

All output relays are set to ones, and the above procedure is repeated with a zero bit being shifted and each channel reset to $FFFF_{16}$ when it is completed.

TEST SECTION 5

This test is identical to Test 4 with the exception that the current image for each 1553 channel is output after each bit shift in a sequence beginning with the channel being modified.

Current version allows exercise of only 16 channel combinations. However, various internal tables can be expanded as desired.

SUPPLEMENTAL SOFTWARE

CRMDOD	DIGITAL OUTPUT DRIVER
CRMDID	DIGITAL INPUT DRIVER

EXAMPLE

Given: 1553 Digital Output Interface connected via the DCB to 1750 DCT with equipment number 8. Output channel addresses are $018 through $01F.

1544 Digital Input Interface connected via the DCB to 1750 DCT with equipment number 9. Input channel addresses are $040 through $04F.

Input channel addresses 048 through 04F are cabled to output channel addresses 018 through 01F via 4 cables CDC P/N 389203XX.

Cable	
	1544 J05 to 1553 J01
	1544 J06 to 1553 J02
	1544 J07 to 1553 J03
	1544 J08 to 1553 J04

All test sections will be run for 10_{16} times, testing the normally open contacts of the relays. Section 3 will use the pattern 1234_{16} for the special pattern.

```
(MI)
CONTROL WORD, PGM NAME
START, TSTREG
BEGIN 1553/1544 TEST
TESTS, RUNS
3E,10          (CR)
OUTPUT DCT WES CODE, INPUT DCT WES CODE
400, 480       (CR)
```

```
OUT CHNL, IN CHNL
18, 48          (CR)
19, 49
1A, 4A
1B, 4B
1C, 4C
1D, 4D
1E, 4E
1F, 4F
FFFF            (CR)
ENTER SPECIAL PATTERN FOR TEST 3
1234            (CR)
TSTREG TEST 4 RUN 0008 1750 STN 0480 EXT REJ
TSTREG TEST 2 RUN 000F 1544 CHL 004F EXT REJ
END 1553/1544 TEST, 0010 RUNS, 0002 ERRORS
```

1544 DIGITAL INPUT INTERFACE TEST ROUTINE

PROGRAM NAME — CRTEXT

TEST MNEMONIC — TSTEXT

PROGRAM FUNCTION — This routine tests the performance of the 1555 Relay or Power Driver Units connected to a 1553 Digital Output Interface and the 1544 Digital Input Interface. Operation of the test requires that each 1555 channel to be tested be connected to a 1544 channel. (1) Thus, various bit patterns are output on the 1559 and input on the 1544; the digital inputs are compared with the output images. Five types of bit configurations are output to the 1559:

1. $FFFF_{16}$ on one channel; all others 0000_{16}.
2. 0000_{16} on one channel; all others $FFFF_{16}$.
3. User input pattern on one channel; all others 0000_{16}.
4. Left-shifting one bit on one channel; all others $FFFF_{16}$.

After each output and input, checks are made for any error indications returned by the drivers. Any errors sensed result in the output of diagnostic messages.

OPERATING INSTRUCTIONS — Once TSTEXT is in control, a message is output on the Standard Output Comment Medium {SOCM} as follows:

```
BEGIN 1555/1544 TEST
TESTS, SWITCH, RUNS
```

The program then enables the Standard Input Comment Medium {SICM} for user keyboard input of three control parameters in the following format:

{Field 1}, {Field 2}, {Field 3} (CR)

---

(1) See Appendix

where: Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

Bit 5 = "1" Do Test 5

The remaining bits are not used.

Field 2 — If non-zero, the normally closed contacts are being tested. If zero, the normally open contacts are being tested. Must be zero for Power Driver Units.

Field 3 — 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test will execute until halted by the user.

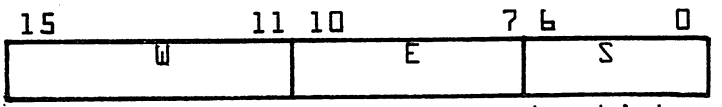
Next, a message is output on the SOCM as follows:

OUTPUT DCT WES CODE, INPUT DCT WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

where Field 1 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1750 Data and Control Terminal {DCT to which the 1553 Digital Output Interface which drives the 1555 Unit is connected.

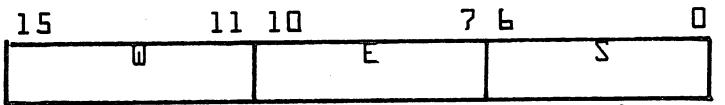


where: W = converter code which must always be zero

E = equipment number of the 1750 DCT

S = station address of the 1750 DCT, always zero.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1750 Data and Control Terminal (DCT) to which the 1544 Digital Input Interface is connected.



where W = converter code which must always be zero.

E = equipment number of the 1750 DCT

S = station address of the 1750 DCT, always zero.

Next, a message is output on the SOCM as follows:

OUT CHNL, IN CHNL

Accordingly, the user must input on the SICM the channel connection information. Each channel set is input separately as shown below:

{Field 1},{Field 2} (CR)

{Field 1},{Field 2} (CR)

. . .

{Field 1},{Field 2} (CR)

FFFF (CR)

Where: Field 1 — 0 to 2 hexadecimal digits representing an allowable 1559 channel address.

Field 2 — 0 to 2 hexadecimal digits representing an allowable 1555{1553} channel address.

FFFF — Input for Field 1 when the user has specified all channel combinations to be tested. A maximum of 16 combinations can be tested at one time.

Upon completion of the number of repeats of the test sequence requested or when halted by the user, the program outputs a message on the SOCM as follows:

END 1555/1544 TEST, hhhh RUNS, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then terminates and exits to the dispatcher.

If test 3 was requested the test halts, before beginning the test sequence, for the user to input the special test pattern as follows:

ENTER SPECIAL PATTERN FOR TEST 3

The message above is output on the SOCM and the user must input one parameter as follows:

{Field 1} (CR)

Where: Field 1 — 1 to 4 hexadecimal digits representing the special test pattern.

ERROR MESSAGE DESCRIPTION

Two types of error messages are output by the program: one for hardware malfunctions and one for discrepancies found between the image output and the image input.

Device reject errors are indicated by a message in the following form:

TSTEXT TEST {1} RUN {2} {3} aaa {4} {5}

where:

{1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} 1555 or 1544 and aaa = CHL

1750 and aaa = STN

{4} If aaa = CHL, the four digit hexadecimal channel address

If aaa = STN, the four digit hexadecimal station address {WES CODE}.

{5} Error description

1555 or 1544

INT REJ — Internal reject-no response from unit

EXT REJ — External reject-unit not ready. Most likely caused by the presence of a synchronization device in the unit.

1750

INT REJ — Internal reject-no response from unit.

EXT REJ — External reject-unit not ready {check protect switch}.

When device errors are detected, no data compare is done.

Whenever the image input differs from the image output, the following message is output:

TSTEXT TEST {1} RUN {2} OUT CHNL {3} IS {4} IN CHNL {5} IS {6}.

where: {1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} Four-digit hexadecimal 1555 channel address.

{4} Four-digit hexadecimal image output.

{5} Four-digit hexadecimal 1544 channel address.

{6} Four-digit hexadecimal image input.

Both type of error messages are output on the Standard List Device {SLD}.

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input the control words and the pair of connected channels. Upon completion of this input, each of the specified tests is conducted in sequence.

Generally, each test involves generating some bit configuration for output on a 1555 channel. A time delay of 8 milliseconds is executed after each output. When the output is accomplished; a check is made for any reject error indications returned by the dirver; a digital input is accomplished on the connected 1544 channel; and a check is made for any reject error indications returned by the 1544 driver. The digital input is compared with the image output; any differences will result in a diagnostic message.

The specific structure of each test is as follows:

TEST SECTION 1

All output relays are zeroed. The image $FFFF_{16}$ is output to a channel. Digital inputs are read from all channels and the inputs are compared to the output images. This procedure is repeated for all channels specified.

TEST SECTION 2

All output relays are set to $FFFF_{16}$. A channel is zeroed. Digital inputs are read on all channels and the inputs are compared to the output images. This procedure is repeated for all channels specified.

TEST SECTION 3

All output relays are zeroed. The special pattern input by the user is output on each channel as in Test 1.

TEST SECTION 4

All output channels are zeroed. Taking each channel in turn, a bit is left-shifted sequentially from positions 0 through 15. The image is output after each shift of the bit, digital inputs are read on all channels, and the inputs are compared to the output images. Each channel is again zeroed once bit 15 has been set and output/input accomplished. This procedure is repeated for each channel specified.

All output relays are set to ones, and the above procedure is repeated with a zero bit being shifted and each channel reset to $FFFF_{16}$ when it is completed.

TEST SECTION 5

This test is identical to Test 4 with the exception that the current image for each 1555 channel is output after each bit shift in a sequence beginning with the channel being modified.

Current version allows exercise of only 16 channel combinations. However, various internal tables can be expanded as desired.

SUPPLEMENTAL SOFTWARE

CRMD0D DIGITAL OUTPUT DRIVER
CRMDID DIGITAL INPUT DRIVER

EXAMPLE

Given: 1555 Relay Unit driven by a 1553 Digital Output Interface connected to a 1750 DCT with equipment code of 8.

There are four 1555 channels, channel addresses 008, 009, 00A and 00B. There are four 1544 channels 000, 001, 002 and 003 which are connected to a 1750 with equipment code of 9. The channels are cabled together via the digital input test box as follows:

Cable from 1544 jack J01 to test box No. 1 jack AI. Cable from 1544 jack J02 to test box No. 2 jack AI. Cable from 1555 jack J07 to test box No. 1 jack A0. Cable from 1555 jack J08 to test box No. 1 Jack B0. Cable from 1555 jack J09 to test box No. 2 jack A0. Cable from 1555 jack J10 to test box No. 2 jack B0.

Cable from 1544 to test box is P/N 389203XX.
Cable from 1555 to test box is P/N 389177XX.

All test sections will be run for 10_{16} times, testing the normally open contacts of the relays. Section 3 will use the pattern 1234_{16} for the special pattern.

```
MI
CONTROL WORD, PGM NAME
START, TSTEXT                CR
BEGIN 1555/1544 TEST
TESTS, SWITCH, RUNS
3E, 0, 10                    CR
OUTPUT DCT WES CODE, INPUT DCT WES CODE
400, 480                     CR
OUT CHNL, IN CHNL
8, 0      CR
9, 1
A, 2
B, 3
FFFF      CR
ENTER SPECIAL PATTERN FOR TEST 3
1234      CR
TSTEXT TEST 1 RUN 0000 1750 STN 0400 INT REJ
TSTEXT TEST 1 RUN 0000 1544 CHL 0000 INT REJ
MI
CONTROL WORD, PGM NAME
STOP, TSTEXT                 CR
END 1555/1544 TEST, 0000 RUNS, 0002 ERRORS
```

PROGRAM NAME CRTSEL

TEST MNEMONIC TSTSEL

PROGRAM FUNCTION The 1583/1584 (FF308/CK4033) Selectric Input/Output Typewriter and Interface Test Routine tests the performance of an IBM Model 735 Selectric I/O typewriter connected to a 1583 selectric typewriter controller. Specifically, the routine determines whether or not the typewriter correctly outputs and inputs all allowable characters in response to commands from the MSOS driver routine. The test routine also checks for proper operation of the color shift feature.

OPERATING INSTRUCTIONS Once TSTSEL is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN SELECTRIC TEST
TEST, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

The remaining bits are not used.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the selected test is to be executed. If bit 15 is set, the test is executed until halted by the user.

Next, a message is output on the SOCM as follows:

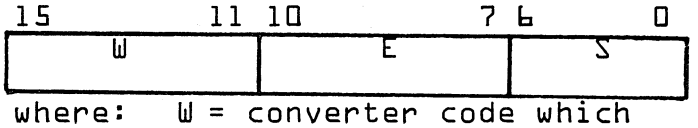
1583 INT LINE, WES CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

where Field 1 — The decimal interrupt line number for the 1583 controller, must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address the 1583 controller for function commands and status requests as shown below.



where: W = converter code which must be zero.

E = equipment number of the 1750 DCT to which the 1583 controller is connected.

S = station address on the DCB of the 1583 controller.

Upon completion of the number of repeats of the test requested or when halted by the user, a message is output on the SOCM as follows:

END SELECTRIC TEST

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

At the completion of each I/O request to the Driver, a check is made for driver detected errors. If an error condition has been detected, the alternate device handler (ALTDEC) error code is decoded to determine the error. Error messages are output on the Standard List Device SLD) as follows:

TSTSEL TIME OUT	No interrupt during driver time limit.
TSTSEL ALARM*	Typer failed to case shift. Typer failed to turn power on. Stall status bit set.
TSTSEL PARITY	Bad character parity on input.
TSTSEL INT REJ	Internal reject, no response from typer interface.
TSTSEL EXT REJ*	External reject, typer controller not ready - typer hung in a cycle or typer no connected to the controller.

*These messages are followed by the hardware status message as follows:

H/W STATUS = hhhh

where hhhh = the last available hardware status.

PROGRAM DESCRIPTION

The following procedure is used to test the typewriter:

TEST SECTION 1

The test outputs the allowable character set repeated until a line of 150 characters is output. The line is first output in red ribbon then in black ribbon. This is repeated the number of times specified.

TEST SECTION 2

The test outputs the message INPUT CHARACTER STRING in red ribbon. The user should input a string of allowable characters followed by a Carriage Return (RETURN). The number of characters input is limited to 150. The driver is monitored by the diagnostic clock, therefore the user must enter a character at least every minute to avoid a Time Out. If a Time Out occurs, the current contents of the buffer are output. When the user enters a RETURN the test outputs the data received from the typewriter. Then the test returns for input.

TEST SECTION 3

The test requests input as in Test 2 but the data is output continuously the number of times specified.

NOTE: On input, the following characters are interpreted as follows:

plus/minus sign	RUB OUT
cent sign	Ignored
backspace	Space
degree sign	Space

SUPPLEMENTAL SOFTWARE

SELECT 1583/1584 DRIVER (Shell Version)
PHYSEL PHYSICAL DEVICE TABLE FOR SELECT DRIVER

EXAMPLE

Given: 1583 controller connected via the DCB to 1750 DCT with equipment code of 8. Station addresses for the 1583 controller are $30 and $31 The interrupt line is 6.

```
(MI)
CONTROL WORD, PGM NAME
LOAD, TSTSEL          (CR)
BEGIN SELECTRIC TEST
TEST, RUNS
2, 5                  (CR)
1583 INT LINE, WES CODE
6, 431                (CR)
TSTSEL ALARM H/W STATUS = 0028
TSTSEL TIMEOUT
END SELECTRIC TEST
```

Documentation for this test will be supplied at a later time.
Software however is currently available.

PROGRAM NAME CRTRL2

TEST MNEMONIC TSTRL2

PROGRAM FUNCTION

This routine tests the performance of the IOM 1555-X Relay Output Unit (DOU) and the IOM 1544-X Digital Input Unit (DIU). Operation of the test requires that each 1555-X card be cabled to a 1544-X card with a special cable with pins connected as shown in Table 1. Cross reference of units tested by the routine is as follows:

Product No.	Equip. No.	Part No.	Card Type
1544-1	DA101B	39842201	2NRT
1544-2	DA101A	39842200	1NKT
1544-3	DA401B	39842203	2NTT
1544-4	DA401A	39842202	2NST
1555-1	DF3A1A	88872300	
1555-2	DF3A1B	88872400	
1555-3	DF3A1A	88872500	

Various bit patterns are output on the 1555-X unit and input on the 1544-X unit; the digital inputs are compared with expected inputs. Normally open relay contacts are connected to bits 0 through 7 of the input unit and normally closed contacts are connected to bits 8 through 15. Five types of bit configurations are output to the 1553-X:

1. FF_{16} on one output; all others 00_{16}.
2. 00_{16} on one output; all others FF_{16}.
3. User input pattern on one output; all others 00_{16}.
4. Left-shifting one bit on one output; all others 00_{16}.
5. Left-shifting a zero bit on one output; all others FF_{16}.

After each output and input, checks are made for errors detected by driver routines. Any errors sensed result in the output of diagnostic messages.

The 1555-X ROU and the 1544-X DIU must be mounted in a 1750-1 Computer Interface Unit or a 1750-2 Computer Interface Expander connected directly to a 1750-1.

OPERATING INSTRUCTIONS

Once TSTRL2 is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN IOM 1544-X/1555-X TEST
TESTS, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

Where Field 1 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

Bit 5 = "1" Do Test 5

The remaining bits are not used.

Field 2 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test will execute until halted by the user.

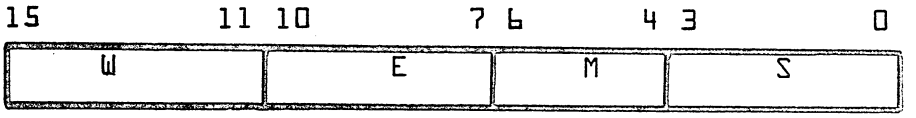
Next the user must input the test configuration information. This is requested by a message output on the SOCM as follows:

```
ENTER - H/W TEST CONFIGURATION INFO
        1555 RELAY OUT  1544 DIGITAL INP
GRP -   WEMS CODE,DASH NO.,WEMS CODE,DASH
```

Accordingly, the user must enter four control parameters on the SICM describing the hardware to be tested. This information is input in the following format:

(Field 1),(Field 2),(Field 3),(Field 4) (CR)

where Field 1 1 to 4 hexadecimal digits representing the 16 bits loaded into the 'Q' register to address the 1555-X ROU card.



where w = converter code which is normally zero

e = equipment number of the computer interface unit (1750-1)

m = module number holding the ROU

s = slot number of the ROU within the module

Field 2 1 digit representing the model number dash number of the 1555-X unit to be tested. Must be in the range of 1 to 3.

Field 3 Same as Field 1 except for the 1544-X DIU card.

Field 4 Same as Field 2 except for the 1544-X DIU card, must be in the range 1 to 4.

If either fields 2 or 4 are in error, (i.e., not in the correct range) a message is output on the SOCM as follows:

TSTRL2 DASH NO. ERROR

and the set of parameters is requested again.

When the set of parameters is input correctly, the operator is requested to put in the next set. The group number is output on the SOCM followed by a request for parameters. This is repeated until the operator inputs $FFFF_{16}$ for the first parameter (1555-X WEMS code) or 16 sets of parameters have been specified.

When the configuration information input is complete the test sequence execution is started.

If test three was requested, the program halts at the beginning to the first pass thru the test sequence for user input of the special test pattern as follows:

ENTER SPECIAL PATTERN FOR TEST 3

The above message is output on the SOCM and user must input one parameter on the SICM as follows:

{Field } 

where Field 1 to 2 hexadecimal digits representing the special test pattern to be used in Test 3.

Upon completion of the number of repeats of the test sequence requested when halted by the user, the program outputs a message on the SOCM as follows:

END IOM 1544-X/1555-X TEST, hhhh RUNS hhhh ERRORS

where hhhh is some hexadecimal number.

The program then terminates and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

Two types of error messages are output by the program; one for hardware rejects and one for discrepancies found between the image output and the image input.

Device rejects are indicated by a message in the following form:

TSTRL2 TEST {1} RUN {2} {3} WEMS CODE {4} {5}

where {1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} 1555 or 1544.

{4} Four digit hexadecimal address in the '@' register {WEMS code} where the reject occurred.

{5} INT REJ Internal reject - no response from unit

or

EXT REJ External reject - unit not ready - Most likely caused by the synchronization circuitry being enabled. Check jumper on card.

When device rejects are detected, no data compare is done.

Whenever the image input differs from the image output, the following message is output:

```
TSTRL2 TEST {1} RUN {2} 1555 ADR {3} IS {4}
                        1544 ADR {5} IS {6}
```

where {1} Decimal number of the test currently being executed.

{2} Hexadecimal number of the current pass through the test sequence.

{3} 1555 ROU WEMS code for the unit data was output to.

{4} Data output to the 1555 ROU.

{5} 1544 DIU WEMS code for the unit data was input from.

{6} Data input from the 1544 DIU.

Both types of message are output on this Standard List Device {SLD}.

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input the control parameters and the test configuration. Upon completion of these inputs each of the specified test sections is conducted in sequence.

Generally, each test section involves generating some bit configuration for output to 1555-X ROU card. A time delay of 4 milliseconds is executed if a 1544-3 or 1555-4 unit is the input unit. When the output is done, a check is made to see if any rejects occurred. An input is done to the 1544-X DIU and the data is compared to the data output. When the input is done, a check is made to see if any rejects occurred. If any rejects occurred or a data compare error was detected, an error message is output on the SLD.

The specific structure of each test is as follows:

TEST SECTION 1

All output units are zeroed. The image FF_{16} is output to one output unit. Inputs are done from all input units and the input image compared to the output image. This procedure is repeated for all units specified.

TEST SECTION 2

All output units are set to FF_{16}. Zero is output to one output unit. Inputs are done from all input units and the input image compared to the output image. This procedure is repeated for all units specified.

TEST SECTION 3

All output units are zeroed. The special test pattern input by the user is output to one output unit as in Test Section 1.

TEST SECTION 4

All output units are zeroed. Taking each output unit in turn, a bit is left-shifted sequentially from position 0 to 15. The image is output after each shift of the bit, the inputs are done from all input units and the images compared. Each channel is again zeroed once bit 15 has been set and the output/input is accomplished. This procedure is repeated for all units specified.

All output units are set to FF_{16}, and the above procedure is repeated with a zero bit being shifted and each channel reset to FF_{16} when it is completed.

TEST SECTION 5

This test section is identical to test Section 4 with the exception that the current image is output for each output unit after each bit shift in a sequence beginning with the channel being modified.

Current version allows exercising of 16 sets only of ROU/DIO unit combination at one time. However, various internal tables can be expanded as desired.

SUPPLEMENTAL SOFTWARE

CRMDOD Digital Output Driver Subroutine
CRMDID Digital Input Driver Subroutine

EXAMPLE:

Given: One 1555-2 ROU plugged into slot number 05 of 1750-1 with equipment number 8 cabled to a 1544-3 plugged into slot number 14 of a 1750-2 module address 3 connected to same 1750-1.

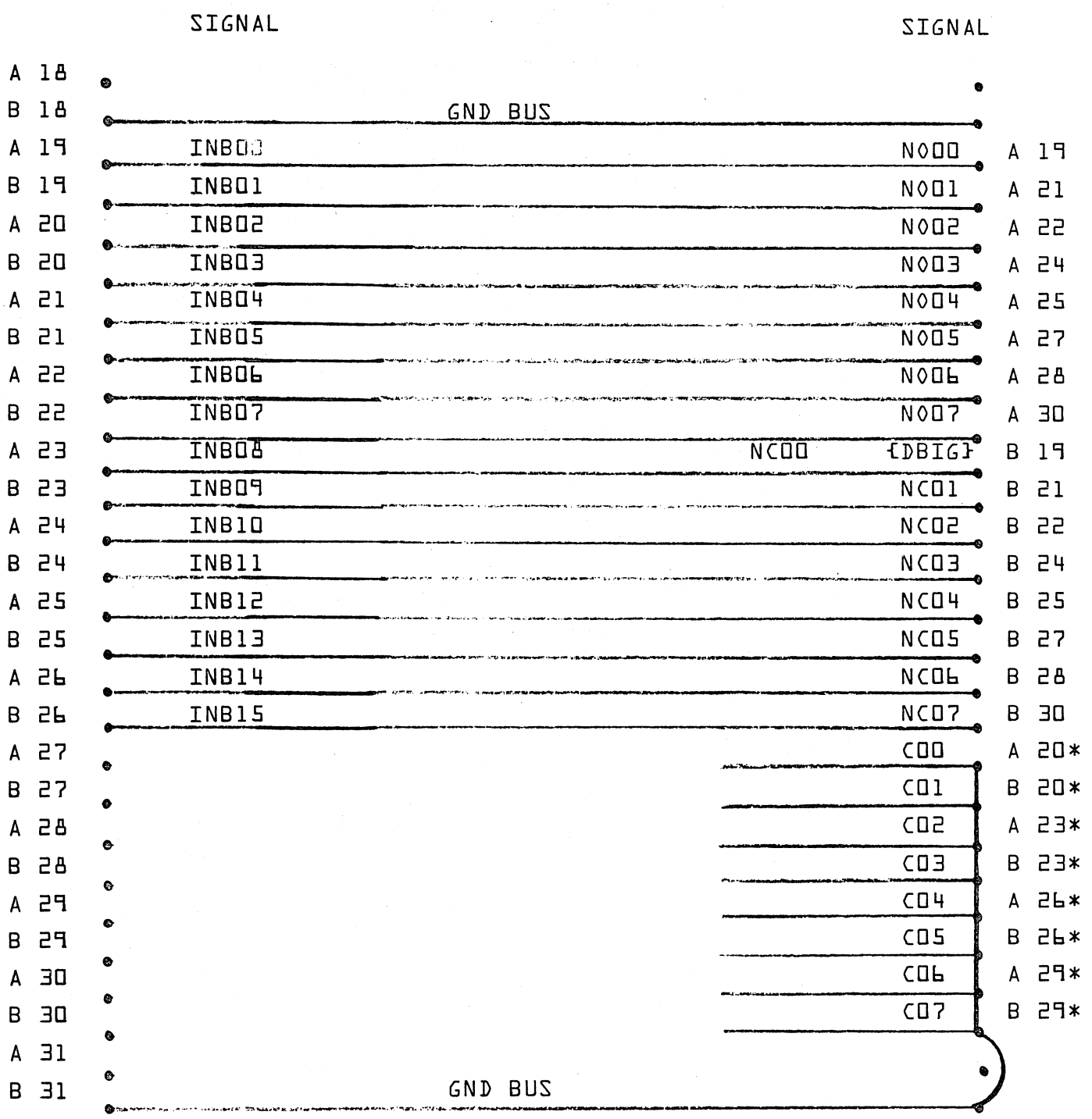
One 1555-1 ROU plugged into slot number 10 of 1750-2 module number 07 connected to a 1750-1 with equipment number A. The 1555-1 is cables to a 1544-4 plugged into slot number 00 of a 1750-1 equipment number C.

Test sections 1, 2, 3 and 4 will be run for 10_{16} passes.

```
(MT)
CONTROL WORD, PGM NAME
START, TSTDIO      (CR)
BEGIN IOM DIGITAL I/O TEST
TESTS, RUNS
1E, 10      (CR)
ENTER - H/W TEST CONFIGURATION INFO
        1553 DIGITAL OUTPUT  1544 DIGITAL INPUT
GRP - WEMS CODE, DASH NO., WEMS CODE, DASH NO.
#01     0405, 2, 043E, 3     (CR)
#02     057A, 6, 0600, 4
#03     FFFF                 (CR)
ENTER SPECIAL PATTERN FOR TEST 3
5678    (CR)
TSTRL2 TEST 3 RUN 0002 1555 WEMS CODE
                            0400 INT REJ
TSTRL2 TEST 5 RUN 000F 1555 ADR 057A
        IS FDFF 1544 ADR 0600 IS FCFF
END IOM 1544X/1555X TEST, 0010 RUNS 0002 ERRORS
```

SPECIAL TEST CABLE
for DF3A1-A/B RELAY OUTPUT UNIT
and DA101-A/B or DA401-A/B DIGITAL INPUT UNIT

from DIU {DIG. IN UNIT} to RELAY OUTPUT UNIT {155}



*Pins A and B, 20, 23, 26 and 29 are tied together and joined to the GND BUS

TABLE 1

Documentation for this test will be supplied at a later time.
Software however is currently available.

Documentation for this test will be supplied at a later time.
Software however is currently available.

PROGRAM NAME CRTSY2

TEST MNEMONIC TSTSY2

PROGRAM FUNCTION

This routine tests the performance of the IOM 1553-X Digital Output Unit (DOU) and the IOM 1544-X Digital Input Unit (DIU) when configured in the synchronous mode. Particular emphasis is placed on synchronizing circuitry testing as the data transfer capabilities can be tested by TSTDIO in the non-synchronous mode. Operation of the test requires that each 1553-X card be cabled to a 1544-X card. Both cards must be jumped into the synchronous mode, the ready signal of each card must be connected to the sync enable signal of the opposite cards. There must be at least one level of inversion of the ready signal. Cross reference of units tested by the routine is as follows:

Product No.	Equip. No.	Part No.	Card Type
1544-1	DA101B	39842201	2NRT
1544-2	DA101A	39842200	1NKT
1544-3	DA401B	39842203	2NTT
1544-4	DA401A	39842202	2NST
1553-1	DA502E	88800100	3SYT
1553-2	DA502F	88800101	3SZT
1553-3	DA502G	88800102	3TAT
1553-4	DA502H	88800103	3TBT
1553-5	DA502J	88800104	4UYT
1553-6	DA502K	88800105	4UZT

The 1553-X DOU and the 1544-X DIU must be mounted in a 1750-1 Computer Interface Unit (CIU) or a 1750-2 Computer Interface Expander (CIE) connected directly to a 1750-1.

OPERATING INSTRUCTIONS

Once TSTSY2 is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN IOM DIGITAL I/O SYNC TEST
TEST, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control parameters in the following format:

(Field 1), (Field 2) (CR)

Where Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

The remaining bits are not assigned.

Field 2 — 1 to 4 hexadecimal digits representing the number of times the test sequence is to be executed. If bit 15 is set, the test will execute until halted by user.

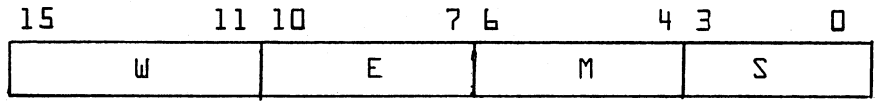
Next, the user must input the test configuration information. This is requested by a message output on SOCM as follows:

```
ENTER - H/W TEST CONFIGURATION INFO
        1553 DIGITAL OUT    1544 DIGITAL INP
GRP   - WEMS CODE,DASH NO.,WEMS CODE,DASH NO.
```

Accordingly, the user must enter four control parameters on the SICM describing the hardware to be tested. This information is input in the following format:

{Field 1},{Field 2},{Field 3},{Field 4} (CR)

Where Field 1 — 1 to 4 hexadecimal digits representing the 16 bits loaded into the 'Q' Register to address the 1553-X DOU card.



where: W = converter code which is normally zero.

E = equipment number of the Computer Interface Unit (1750-1).

M = module number holding the COU.

S = slot number of the DOU within the module.

Field 2	1 digit representing the model number dash number of the 1553-X unit to be tested. Must be in range of 1 to 6.
Field 3	Same as Field 1 except for the 1544-X DIU card.
Field 4	Same as Field 2 except for the 1544-X DIU card. Must be in the range of 1 to 4.

If either fields 2 or 4 are in error, (i.e. not in the correct range) a message is output on the SOCM as follows:

TSTSY2 DASH NO. ERROR

and the set of parameters is requested again.

When the set of parameters is input correctly, the operator is requested to put in the next set. The group number is output on the SOCM followed by a request for parameters. This is repeated until the operator inputs $FFFF_{16}$ for the first parameter (1553-X WEMS code) or 16 sets of parameters have been specified.

When the configuration information input is complete, a check is made for Test 2 requested. If requested, the following message is output on the SOCM:

1553 COMMON SYNC INT LINE

The user must enter one parameter on the SICM in the following format:

(Field) (CR)

Where Field the decimal interrupt line number for the 1553-X DOU cards. All cards under test must have the same interrupt line number and all DOU's connected to that interrupt line must be specified for testing. Must be in the range of 2 to 15.

The interrupt line input is checked for correct range and to determine if it is currently busy. If the line number is not in range or is currently busy, the following message is output on the SOCM:

TSTSY2 INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if this error is repeated three times in succession, the test is terminated.

A check is made for Test 3 requested, and if so, the following message is output on the SOCM:

1544 COMMON SYNC INT LINE

The user must enter one parameter on the SICM for the 1544-X DIU interrupt line. The range must be 2 to 15 and the interrupt line can not be the same as the 1553-X if both Tests 2 and 3 are requested. The interrupt line is checked for error as above.

A check is then made for Bit 15 ='1' of the TESTS parameter. If equal to one, the following message is output on the SOCM:

SPECIAL DATA PATTERN

Accordingly, the user must enter on the SICM one control parameter to specify the hexadecimal data pattern to be used for all I/O operations for the test. It is input in the format:

{Field} (CR)

where Field is 1 to 4 hexadecimal digits representing the data pattern to be used as described above.

Upon completion of the number of repeats of the test sequence requested, or when halted by the user, the program outputs a message on the SOCM as follows:

END IOM SYNC TEST, hhhh RUNS, hhhh ERRORS

where hhhh is some hexadecimal number

The program then terminates and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

All test sequences are monitored for errors and when error conditions are detected, a message is output on the Standard List Device (SLD). All error messages are preceeded by the following message header:

TSTSY2 TEST d RUN hhhh WEMS wwww

where d is the current test section being executed

hhhh is the hexadecimal number representing the current pass through the test sequence.

wwww is the WEMS code of the sync channel under test or its corresponding module flag status address.

This message header is followed by one of the following descriptive error messages:

INTERRUPT FLAG NOT SET

This message indicates that the module status did not have a ready bit set, for the WEMS address specified, when it should have been set.

INTERRUPT FLAG SET

This message indicates that the module status had a ready bit set, for the WEMS address specified, when it should not have been set.

REPLY ERROR

This message indicates that a REPLY was received from the specified WEMS address when an EXTERNAL REJECT was expected.

EXTERNAL REJECT

This message indicates that an EXTERNAL REJECT was received from the specified WEMS address when a REPLY was expected.

INTERNAL REJECT

This message indicates that no response was received from the specified WEMS address.

GHOST INTERRUPT

This message indicates that an interrupt was received but its origin could not be identified (no interrupt flags were set).

NO INTERRUPT

This message indicates that no interrupt was received when one was expected.

DATA ERROR ACTUAL hhhh EXPECTED hhhh

This message indicates a data error occurred on the specified input WEMS address, hhhh is some hexadecimal value.

PROGRAM DESCRPTION

Before the test sequence can be conducted, the user must input the control parameters and the test configuration. Upon completion of these inputs, each of the specified test sections is conducted in sequence.

All I/O operations are monitored for correct H/W response. If the input unit is a 1544-3 or 1544-4 DIU, a 418 millisec delay is executed between output commands and checks for expected input unit response. All error conditions are reported via messages to the SLD.

TEST SECTION 1 - READY FLAG/REJECT

All input units are read to insure that units are reset. Each address set is then taken in turn. The output unit ready flag should be set. The input unit ready flag should not be set. An output is done to the output unit and a reply should occur. The input unit flag should not be set. The output unit flag should be set. An output is done again to output unit and an external reject should occur. An input is done to the input unit and a reply should occur. The data is compared to output data and corrected for signal conditioning type. The input unit flag should not be set. The output unit flag should be set. An input is done again to input unit and an external reject should occur. This sequence is repeated for all address sets specified.

TEST SECTION 2 - OUTPUT UNIT INTERRUPT

All output units are written to ensure a reset condition. The output unit interrupt line is then enabled. An input is done to one input unit. A check is made for interrupt received. All output units are checked for proper H/W response when interrupt received; all units except unit with interrupt should have given an EXTERNAL REJECT to an output command; the unit with interrupt should have given a REPLY. The ready flag for each unit is checked for proper status. Each output unit is processed as described.

TEST SECTION 3 - INPUT UNIT INTERRUPT

All input units are read to insure a reset condition. The input unit interrupt line is then enabled. An output is done to one output unit. A check is made for interrupt received. All input units are checked for proper H/W response when the interrupt was received; all units except unit with the interrupt should have given an EXTERNAL REJECT to an input command; the unit with the interrupt should have given a REPLY. The ready flag for each unit is checked for proper status. Each input unit is processed as described.

SUPPLEMENTAL SOFTWARE

CRMDOD Digital Output Driver Subroutine
CRMDID Digital Input Driver Subroutine

EXAMPLE:

Given: One 1553-1 DOU plugged into slot number 01 of a 1750-1 with equipment number 8 and cabled to a 1544-1 DIU plugged into slot number 02 of same 1750-1.

One 1553-2 DOU plugged into slot number 05 of the above 1750-1 cabled to a 1544-3 DIU plugged into slot number 14 of a 1750-2 module address 3 connected to same 1750-1.

One 1553-6 DOU plugged into slot number 10 of a 1750-2 module address 7 connected to a 1750-1 with equipment number A. The 1553-6 is cabled to a 1544-4 plugged into slot number 15 of a 1750-1 with equipment number C.

The 1553-X DOU's are connected to interrupt line 15.

The 1544-X DIU's are connected to interrupt line 14.

Test sections 1, 2 and 3 will be run for 50_{16} passes.

A special data pattern will be requested.

```
MI
CONTROL WORD, PGM NAME
START, TSTSY2    (CR)
BEGIN IOM DIGITAL I/O SYNC TEST
TESTS, RUNS
800E, 50     (CR)
ENTER - H/W TEST CONFIGURATION INFO
        1553 DIGITAL OUT    1544 DIGITAL INP
GRP - WEMS CODE, DASH NO., WEMS CODE, DASH NO.
  #01 0401, 1, 0402, 1     (CR)
  #02 0405, 2, 043E, 3     (CR)
  #03 0574, 6, 060F, 4     (CR)
  #04 FFFF    (CR)
1553 COMMON SYNC INT LINE
15    (CR)
1544 COMMON SYNC INT LINE
14    (CR)
SPECIAL DATA PATTERN
1357  (CR)
TSTSY2 TEST 1 RUN 0037 WEMS 043E EXTERNAL REJECT
TSTSY2 TEST 2 RUN 0037 WEMS 043E INTERRUPT FLAG NOT SET
TSTSY2 TEST 3 RUN 004A WEMS 060F NO INTERRUPT
TSTSY2 TEST 4 RUN 004E WEMS 0402 GHOST INTERRUPT
END IOM DIGITAL I/O SYNC TEST, 0050 RUNS, 0004 ERRORS
```

PROGRAM NAME CRTMCD

MNEMONIC NAME TST MCD

PROGRAM FUNCTION The 1833-4/1866-1X Test Routine is a series of test designed to exercise and determine the performance of the 1833-4 Cartridge Disk Drive Controller and the 1866-12 or 1866-14 Cartridge Disk Drives in their various modes of operation using the MSOS driver. The user must specify the dimensions of the disk section to be tested and the particular operations to be performed as part of the test sequence. The program exercises and monitors the performance of the following operations:

1. Read/Write head switching.
2. Core-to-disk transfers of information(1) in block lengths 2048_{10} words.
3. Disk-to-core transfers of information(1) in block lengths 2048_{10} words.
4. Transfer of information from a specified core/disk location to a specified disk/ core location
5. Read head positioning (see operation).

Any errors sensed during the conduct of a test will cause appropriate disgnostics to be output on the Standard List Device (SLD. The program will diagnose any of the following discrepancies:

1. Alteration of information during core-to-disk or disk-to-core transfers.
2. Transferred information displaced from destination locations.

---

(1) Information includes four worst patterns ($9555, $6AAA, $5A5A and $A5A5), all ones, and pseudorandom bit patterns.

3. Lost data, address, seek, defective track and storage parity errors during write operation.

4. Lost data, address, seek, protect fault, defective track, check word and storage parity errors during read operation.

OPERATING INSTRUCTIONS

Once TSTMCD is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

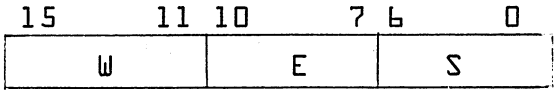
```
BEGIN 1733-2/856-X MULTIPLE
CARTRIDGE DISK DRIVE TEST
1733-2 INT LINE, WES CODE
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control words in the following format:

(Field 1), (Field 2) (CR)

Where: Field 1 the decimal interrupt line number for the 1733-2 controller, must be in the range of 2 to 15.

Field 2 1 to 4 hexadecimal digits representing the 16 bits loaded into the "@" register to address the 1733-2 controller as shown below:



Where: W = converter code which must be zero.

E = equipment number of the 1733-2 controller

S = station address - set to one by test routine.

The interrupt line input is checked for correct range and if currently busy (in use). If the line number is not in range or is currently busy, the following message is output on the SOCM:

```
TSTMCD INTERRUPT ASSIGNMENT ERROR
```

The parameters are then requested again, if the error is repeated three times in succession, the test is terminated.

Following the correct input of the interrupt line number, the following message is output on the SOCM:

UNITS TO BE TESTED

Accordingly, the user must enter one control parameter on the SICM in the following format:

{Field} (CR)

Where Field 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 0 = "1" Test Unit 0

Bit 1 = "1" Test Unit 1

Bit 2 = "1" Test Unit 2

Bit 3 = "1" Test Unit 3

The remaining bits are not used.

At least one bit must be set or the parameter is requested again.

If more than one bit was set, indicating that more than one unit will be tested, the following message will be output on the SOCM:

ARE PARAMETERS FOR ALL UNITS THE SAME?

Accordingly the user must enter one of the following via the keyboard of the SICM:

YES (CR) or NO (CR)

If YES is entered, the parameters for all units will be the same and the parameters will only be requested once. If NO is entered, the parameters will be requested for each unit to be tested.

Next the user will be requested to input the test parameters. The following message will be output on the SOCM:

PARAMETERS FOR UNIT a
TYPE, TESTS, BEG SEC,END SEC,RUNS

Where a = 0, 1, 2 or 3 depending on the units to be tested. If YES was entered above "a" will equal ALL

The SICM will then be enabled for user keyboard input of five control words in the following format:

{Field 1}, {Field 2}, {Field 3}, {Field 4}, {Field 5} (CR)

When: Field 1 is one digit as follows

Zero for 856-2 or 856-12 single density disk, maximum sector address is $5BFB, first sector on fixed disk is $2DFE.

Non Zero for 856-4 or 856-14 double density disk, maximum sector address as $B7F7, first sector address on fixed disk is $5BFC.

Field 2 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

Bit 5 = "1" Do Test 5

Bit 6 = "1" Do Test 6

The remaining bits are not assigned.

Field 3 1 to 4 hexadecimal digits representing the disk sector address at the beginning of test area.

Field 4 1 to 4 hexadecimal digits representing the disk sector address at the end of test area.

Field 5 1 to 4 hexadecimal digits representing number of times the test sequence is to be run. If bit 15 is set, the test will execute until halted by the user.

If the beginning disk address is larger than the ending disk address or the ending disk address exceeds the size of the disk, the message below is output on the SOCM and the parameters are requested again.

```
TSTMCD SEC ADD ERR
```

Following acceptable input of test parameters the test sequence will begin.

Each unit to be tested will output the following message on the SOCM:

```
TSTMCD UNT a BEGIN
```

Where a = 0, 1, 2, or 3

When the test ends for a particular unit the following message is output on the SOCM:

```
TSTMCD UNT a BEGIN
```

Where a = 0, 1, 2, or 3

When the test ends for a particular unit the following message is output on the SOCM:

```
TSTMCD UNT a END,hhhh RUNS,hhhh ERRORS
```

Where hhhh is some hexadecimal number

When all units have completed, the following message is output on SOCM:

```
END 1733-2/856-X TEST
```

The program then clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

All error messages output by the program are output on the Standard List Device (SLD) and are of the same general format.

```
TSTMCD UNT a TEST (1) RUN (2) (3) (4) XFER
H/W ADDR (5)
```

Where: a is 0, 1, 2 or 3

(1) Decimal number of the test currently being executed

(2) Hexadecimal number of the current pass through the test sequence.

(3) One of the following error messages:

NOT RDY	Disk unit not ready. Can also result from a reject
COMP ERR	Data comparison error. An additional message is also output describing the location and actual data error. (The direction of transfer is deleted from this message).
LOST DATA	A second word was received from the drive unit before the first word was transferred to core and then an attempt was made to transfer a word to core.
PARITY	Core storage parity error detected during data transfer.
PROTECT	A data transfer was initiated from unprotected core to or from a protected area.
ADR ERR	An illegal disk address was received by the controller.
DRIVE SEEK ERROR	Drive unit detected a seek error.
CONTROLLER SEEK ERROR	1739-1 controller detected a seek error condition.
TIME OUT	1739-1 controller did not interrupt when expected.
NO COMP	Error detected during a hardware data compare operation. Should never be output as driver does not perform this operation.
CHKWRD ERR	Checkword on disk pack does not equal that calculated by the controller during data transfer.

INT REJ — Internal reject was received. 1739-1 did not respond to I/O comman.

EXT REJ — External reject was received. 1739-1 sent a reject to an I/O command.

REG. STATUS ERROR — One of the following registers did not agree with what was expected:

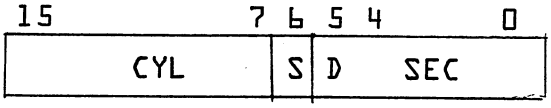
CURRENT WORD ADDRESS
CONTROLLER CYLINDER ADDRESS
DRIVE CYLINDER ADDRESS

An additional message is output to describe the complete error {See description below}.

{4} Direction of transfer

D-C — Disk to core
C-D — Core to disk

{5} Actual disk hardware address {hexadecimal} at the beginning of the data transfer.



Where:

CYL — is the drive cyclinder address in the decimal range {value as hex}.
856-2/12
0 to 202
0 to 405
856-4/14

S — is the surface on the disk.

"0" = upper surface
"1" = lower surface

D — is the disk.

"0" = removable
"1" = fixed

SEC — is the drive sector address in the decimal range 0 to 28.

In the case of a comparison error (COMP ERR), additional messages are output in the following format:

WORD (1) WAS (2) IS (3)

where: (1) Hexadecimal number of the word within the sector where the contents were altered.

(2) Bit pattern sent to that word.

(3) Bit pattern returned from that word.

When the comparison test has been completed and at least one or more comparison errors were detected, a message is output on the SLD as follows:

TSTCDD COMP ERR TOTAL (1)

where: (1) Hexadecimal total of comparison errors detected in the block being tested (range 1 - 800).

In the case of a register status error (REG. STATUS ERROR) an additional message is output on the SLD following the first error message. The format is:

(1) ADDRESS STATUS-ACTUAL (2) EXPECTED (3)

where (1) is one of the following:

CURR WORD for a current word address register error

CNTLR CYL for a controller cylinder address register error

DRIVE CYL for a drive cylinder address register error

(2) The actual register contents

(3) The expected register contents

A typecal error printout would be as follows

```
TSTMCD UNIT0 TEST 4 RUN 0013 PARITY D-C XFER H/W ADDR 0104
TSTMCD UNIT0 TEST 4 RUN 0013 COMP ERR H/W ADDR 0104
WORD 0020 WAS B5A2 IS B1A2
TSTMCD COMP ERR TOTAL 0001
TSTMCD UNIT0 TEST 4 RUN 0013 REG. STATUS ERROR
    D-C XFER H/W ADDR 0104
CURR WORD ADDRESS STATUS - ACTUAL 2F42 EXPECTED 2F5B
```

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input six control words which specify the desired test sequence, the beginning sector address, the ending sector address, the number of times to repeat the test sequence, the controller interrupt line number and the controller WES code.

The test addresses the disk as a word addressable device (2-word address as in the 1751 Drum) instead of sector addressable (96 words/sector). Accordingly, the sector addresses are intially converted to two-word addresses which are used throughout the test. When an error is encountered, the current two-word address is converted to a hardware address (as is output to this disk controller for a load address function) plus some word number if appropriate. The resultant addresses are output in the diagnostic message.

The program jumps to each of the tests (See pages 28-10, 28-11 desired by the user and outputs appropriate diagnostic messages when errors are detected. The following procedures are common to each test.

Information to be written on the disk is loaded into a fixed 2048_{10} word buffer. The variable parameters of the disk transfer call sequence are specified, and a Monitor request is executed to accomplish the transfer of the specified number of words to the specified disk area. The beginning core address for the transfer is fixed for all tests. The block of information generated for a particular test is repeatedly transferred until it has been written throughout the specified disk test area. Once this has been accomplished each block of information is read from the disk into the buffer, and the original information if regenerated and compared to that contained in the buffer. Any discrepancy between the original information and that returned from the disk results in the output of a comparison error message on the SLD.

At the completion of each transfer request, the status returned by the disk is examined for any error bits set. Any error condition results in the output of a diagnostic message that indicates the actual h/w address at which the transfer began. Any error condition will cause the transfer to be repeated once. In the case of a parity error, a comparison check is made prior to the re-execution of the transfer. (Note: the comparison check is not executed if the parity error occured while conducting Test 4. The transfer is, however, re-attempted.)

Upon completion of the second transfer, the program checks the disk status, outputs diagnostic messages if any errors still exist, and resumes the normal sequence. At this point, all tests conduct a comparison check. The comparison test of the original patterns and the returned patterns is conducted throughout each transferred block even though comparison errors exist throughout the block. Comparison error messages are suppressed after the third error in a block; a tally of comparison errors for that block is computed and printed out when the comparison test is completed but only when at least one or more comparison errors were sensed in that block.

When the program completes a pass through all specified tests, it determines whether or not the test sequence should be terminated either because the test sequence has repeated the specified number of times or because the user has set the stop flag (i.e. STOP/TSTCDD). Also, the stop flag is checked after each disk transfer.

REST SECTION 1

Transfer 2048_{10} Word Blocks of Worst Bit Patterns

Four worst patterns are used in this test: 9555_{16}, $6AAA_{16}$, $5A5A_{16}$, and $A5A5_{16}$. The 2048_{10} word buffer is loaded with a worst pattern and transferred to the disk until it is completely loaded. The disk is read a block at a time, and each word of the 2048_{10} word block is compared with the original pattern. This procedure is repeated for each of the four worst patterns.

TEST SECTION 2

Transfer 2048_{10} Word Blocks Containing all Ones

The 2048_{10} word buffer is filled with "1's" and transferred to the disk until it is completely loaded. The disk is read a block at a time, and each block of information is checked for all "1's."

TEST SECTION 3

Transfer 2048_{10} word Blocks of Pseudo-Random Bit Patterns

The 2048_{10} word buffer is filled with randomly generated bit patterns and repeatedly transferred to the disk until it is completely loaded. Each block is read and compared with the original information a block at a time. A new set of random numbers is generated for each pass through this block.

TEST SECTION 4

Transfer Pseudo-Random-Length Blocks of Pseudo-Random Bit Patterns

The 2048_{10} word buffer is loaded with randomly generated bit patterns; then, successive block lengths are randomly generated, and a block is transferred for each length generated. The blocks are written on the disk so that each block begins directly following the succeeding one. When the test is completed, the random information is read a block at a time and compared with the original patterns. A new set of random patterns and random block lengths are generated for each pass through this test.

TEST SECTION 5

Transfer 2048_{10} Word Blocks Containing All Ones

The 2048_{10} word buffer is filled with "1's" and transferred to the disk until it is completely loaded. This phase is repeated ten times. The buffer is zeroed and transferred to the disk until it is completely loaded. The disk is read a track at a time, and each block is checked for all zeros.

TEST SECTION 6

Transfer 2048_{10} Word Blocks Containing Worst Pattern 9555_{16} to Random Addresses

The 2048_{10} word buffer is filled with the worst pattern 9555_{16} to Random Addresses

The 2048_{10} word buffer is filled with the worst pattern 9555_{16}. The block is then transferred to and read from the disk at randomly generated addresses. Each block is checked for 9555_{16} throughout.

NOTES:

To convert to or from sector addressing to hardware addressing, the following should be remembered:

96 words (16 bit) per sector
29 sectors per track
2 tracks per cylinder
203 cylinders per disk (856-2/12)
406 cylinders per disk (856-4/14)
2 disks per drive

Normally, Disk 0 is the removable disk and disk 1 is the fixed disk.

The test routine considers the drive with two disks as one continuous medium.

For the 856/2/12 disk, there are 11774_{10} sectors on a disk therefore, the highest sector address on disk 0 is $2DFD_{16}$, the lowest sector address on disk 1 is $2DFE_{16}$ and the highest sector address on disk 1 is $5BFB_{16}$.

For the 856-4/14 disk, there are 23548_{10} sectors on a disk therefore, the highest sector address on disk 0 is $5BFB_{16}$, the lowest sector address on disk 1 is $5BFC_{16}$ and the highest sector address on disk 1 is $B7F7_{16}$.

Run time (approximate) for all disk sectors, all test sections is 3 1/2 hours (856-4/14).

SUPPLEMENTAL SOFTWARE

PDTMCD Physical Device Tables for D17332
D17332 MSOS4.X driver for 1733-2/856-X/856-1X.

EXAMPLE

Given: 1733-2 Controller with two 856-14 drives units 0 and 1 and one 856-12 drive, unit 2. Controller has an equipment code of 3 and an interrupt line of 3.

```
(MI)

CONTROL WORD,PGM NAME
LOAD,TSTMCD
BEGIN 1733-2/856-X MULTIPLE
CARTRIDGE DISK DRIVE TEST
1733-2 INT LINE,WES CODE
3,181   (CR)
UNITS TO BE TESTED
3   (CR)
ARE PARAMETERS FOR ALL UNITS THE SAME?
YES   (CR)
PARAMETERS FOR UNIT ALL
TYPE,TESTS,BEG SEC,END SEC,RUNS
1,2,0,B7F7,1   (CR)
TSTCCD UNT 0 BEGIN
TSTCCD UNT 1 BEGIN
TSTCCD UNT 0 END,0001 RUNS,0000 ERRORS
TSTCCD UNT 0 END,0001 RUNS,0000 ERRORS
END 1733-2/856-X TEST
(MI)
CONTROL WORD,PGM NAME
START,TSTMCD   (CR)
BEGIN 1733-2/856-X MULTIPLE
CARTRIDGE DISK DRIVE TEST
1733-2 INT LINE,WES CODE
3,181   (CR)
UNITS TO BE TESTED
7   (CR)
ARE PARAMETERS FOR ALL UNITS THE SAME?
NO   (CR)
PARAMETERS FOR UNIT 0
TYPE,TESTS,BEG SEC,END SEC,RUNS
1,2,0,B7F7,4   (CR)
PARAMETERS FOR UNIT 1
TYPE,TESTS,BEG SEC,END SEC,RUNS
1,40,0,5BFB,100   (CR)
PARAMETERS FOR UNIT 2
TYPE,TESTS,BEG SEC,END SEC,RUNS
0,42,0,2DFD,1   (CR)
TSTMCD UNT 0 BEGIN
TSTMCD UNT 1 BEGIN
TSTMCD UNT 2 BEGIN
TSTMCD UNT 2 END,0001 RUNS,0000 ERRORS
TSTMCD UNT 0 END,0004 RUNS,0000 ERRORS
TSTMCD UNT 1 END,0100 RUNS,0000 ERRORS
END 1733-2/856-X TEST
```

Documentation for this test will be supplied at a later time.
Software however is currently available.

PROGRAM NAME CRTAD4

TEST MNEMONIC TSTAD4

PROGRAM FUNCTION

This routine tests the performance of IOM 1501-10, -11/1525-3 Solid State Analog Input Subsystem. Generally, the routine obtains inputs from a sequence of 1- to 8- channel sets, repeats a specified number of times, compares the actual to the expected counts, and generates a double-precision histogram which allows a maximum count of 9,999,999 for each error counter.

In order to conduct the test, the user must provide the expected full-scale value for each mux address being tested. This is most conveniently accomplished using the Analog Input Test Box (Control Data Part No. 39007700) [1] which provides variable DC inputs to each mux address of a sequence of 8-mux address sets. With the test box, the user can apply the desired voltage to each of the mux addresses; then, when requested by the test routines he can enter the full scale reading (%) expected for each mux address. This information is converted by the program to expected counts (given that it has previously received correct calibration data). The expected counts are compared to actual counts to produce a histogram of errors.

After each input, checks are made for any error indications returned by the driver. Any errors indicated result in the output of diagnostic messages.

OPERATING INSTRUCTIONS

Once TSTAD4 is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN ADC NO. 4 TEST
BEG CHL INDX, END CHL INDX, RUNS
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of three control parameters in the following format:

(Field 1), (Field 2), (Field 3) (CR)

1 See Appendix

Where: Field 1 — 2 hexadecimal digits representing the lowest mux address to be tested.

Field 2 — 2 hexadecimal digits representing the highest mux address to be tested.

Field 3 — 1 to 4 hexadecimal digits representing the number of times each mux address is to be multiplexed. If bit 15 is set, the test will execute until a maximum count of 9,999,999 is recorded in any error cell or until halted by the user.

If the ending mux address input is less than the beginning mux address input, the message below is output on the SOCM and the parameters are requested again.

TSTAD4 ADR ERR

Finally, if zero runs were input or the runs field left brank, no message is output but the parameters are requested again.

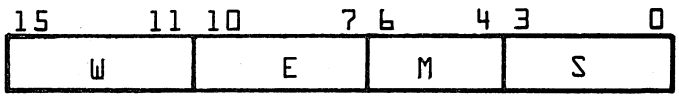
Next, a message is output on the SOCM as follows:

1525-3 WEMS CODE

Accordingly, the user must enter one control parameter on the SICM in the following format:

{Field} (CR)

where: Field — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the 'Q' register to address 1525-3 ADC.



where W = converter code which must always be zero.

E = equipment code of the Computer Interface Unit

M = module address of the module holding the 1525-3 ADC.

S = slot address of 1525-3 within the module.

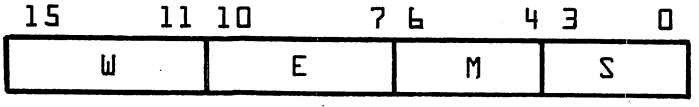
Next a message is output on the SOCM as follows:

MUX ADDRESS, NUMBER OF CHNLS

Accordingly, the user must enter two control parameters on the SICM in the following format:

{Field 1}, {Field 2} (CR)

Where Field 1 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the Q register to address the channels of that multiplexer.



where W = converter code which must be zero.

E = equipment code of the Computer Interface Unit.

M = module address of the module holding the 1501-10

S = slot address of the 1501-10 within the module

Field 2 — 1 or 2 hexadecimal digits defining the number of channels associated with the 1501 in the address above. If 1501-10 only the number is 8, if 1501-10 1501-11 the number is 10_{16}.

After the parameters are input, the operator is signalled to put in the next set. The group number is output on the SOCM to request new parameters. This is repeated until the operator inputs $FFFF_{16}$ for the first parameter (Field 1) or 16 sets of parameters have been specified.

NOTE: The channel indexes input previously are determined by the configuration entered above. Channel index zero is the first channel of the first multiplexer whose address has been entered above. Indexes are consecutive through the channels as entered with the last index being the last channel of the multiplexer whose address was last entered.

Next, a message is output on the SOCM as follows:

SCALE, CK POINT DELAY

Accordingly, the user must enter three control parameters on the SICM in the following format:

{Field 1}, {Field 2}, {Field 3} (CR)

Where: Field 1 — 1 to 4 hexadecimal digits representing the histogram scale factor The expected counts are subtracted from the actual counts input and the result is divided by a non-zero scale factor to product the scaled conversion error recorded in the histogram.

Field 2 — If the field is non-zero, then whenever the scaled conversion error is greater than +7 or less than -7 a message is output indicating the mux address which was out of range. {see error description page

Field 3 — 1 to 4 hexadecimal digits representing the number of 10 millisecond delays to be executed between converting each set of points.

Next, a message is output on the SOCM as follows:

% FULL SCALE

The user must then enter eight sets of parameters to describe the expected counts and gain for each mux addres set. The request for each parameter set is preceeded by a message. The message and parameters request are as follows:

POINT X {Field 1} (CR)

Where: X — The number 1 to 8 for mux address sets 1 to 8.

Field 1 — 1 to 4 hexadecimal digits representing the expected percent full scale from the mux address s This is a signed value {i.e. if negative the complement of the percent full is entered}.

If the expected full scale value is unkown, the user may enter $8000 for Field 1 which signals to the test routine to use the first value input from the mux address set as the value for expected counts.

If seven or less mux addresses are requested in the first parameter request, then the mux address set information request and the histogram are abbreviated accordingly. (i.e. if 000 and 002 are input for the beginning and ending mux addresses respectively, then mux address set information is requested only for points 1, 2 and 3).

Upon completion of the number of times each mux address was requested to be multiplexed or when halted by the user, the resultant histogram is output (if the SKIP SWITCH is not set) on the Standard List Device (SLD) followed by a message on the SOCM as follows:

END ADC NO. 4 TEST, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then terminates and exits to the dispatcher.

Figure 30-1 Page 30-10 is an example of the parameter input and resultant histogram.

ERROR MESSAGE DESCRIPTION

When error conditions are detected, messages are output on the SLD to describe the error condition. These messages are of one general type as shown below:

TSTAD4 MUX ADR {1} {2}

where: {1} Four-digit hexadecimal mux address

{2} Any one of the following messages

ANALOG INDEX ERROR	Analog channel index entered exceeds maximum channel index for the configuration that was input.
1536 INT/EXT REJ	either an internal or external reject was received when doing an I/O instruction to the 1536-E controller
1525-3 INT/EXT REJ	either an internal or external reject was received when doing an I/O instruction to the 1525-3 ADC.
OVER RANGE	value input from ADC for mux address stated was the maximum value that the ADC could output.
UNDER RANGE	value input from ADC for mux address stated was the minimum value that the ADC could output.
CK RELAY	Value of the scaled conversion error is outside the range of the histogram (i.e., greater than +7 or less than -7). This message is determined by the test and is not counted as an error.

If the expected full scale value is unkown, the user may enter $8000 for Field 1 which signals to the test routine to use the first value input from the mux address set as the value for expected counts.

If seven or less mux addresses are requested in the first parameter request, then the mux address set information request and the histogram are abbreviated accordingly. (i.e. if 000 and 002 are input for the beginning and ending mux addresses respectively, then mux address set information is requested only for points 1, 2 and 3).

Upon completion of the number of times each mux address was requested to be multiplexed or when halted by the user, the resultant histogram is output (if the SKIP SWITCH is not set) on the Standard List Device (SLD) followed by a message on the SOCM as follows:

END ADC NO. 4 TEST, hhhh ERRORS

where hhhh is some hexadecimal number.

The program then terminates and exits to the dispatcher.

Figure 30-1 Page 30-10 is an example of the parameter input and resultant histogram.

EXAMPLE

```
MI
CONTROL WORD, PGM NAME
LOAD, TSTAD4    CR
BEGIN ADC NO. 4 TEST
BEG CHL INDX, END CHL INDX, RUNS
0, 7, FFF    CR
MUX ADDRESS, NUMBER OF CHNLS
NO. 1    481, 10
NO. 2    482, 10
NO. 3    483, 10
NO. 4    FFFF
   |
   |
   |
   |
   |
NO. 16
1525-3 WEMS CODE
48C      CR
SCALE, CR POINT, DELAY
1, 1, 0 CR
% FULL SCALE, GAIN
POINT 1 0, 1   CR
POINT 2
POINT 3
POINT 4
POINT 5
POINT 6
POINT 7
POINT 8 0, 1   CR

TSTAD4 HISTOGRAM OF RESULTS
SCALE FACTOR 0001 ADDR 0000-0007 RUNS 00004095
```

POINT	1	2	3	4	5	6	7	8
EX CNTS	0000	0000	0000	0000	0000	0000	0000	0000
GT	0	0	0	0	0	0	0	0
+7	0	0	0	0	0	0	0	0
+6	0	0	0	0	0	0	0	0
+5	0	0	0	0	0	0	0	0
+4	0	0	0	0	0	0	0	0
+3	0	0	0	0	0	0	0	0
+2	0	0	0	0	0	0	0	0
+1	0	0	0	0	0	0	0	0
0	4095	4095	4095	4095	4095	4095	4095	4095
-1	0	0	0	0	0	0	0	0
-2	0	0	0	0	0	0	0	0
-3	0	0	0	0	0	0	0	0
-4	0	0	0	0	0	0	0	0
-5	0	0	0	0	0	0	0	0
-6	0	0	0	0	0	0	0	0
-7	0	0	0	0	0	0	0	0
LT	0	0	0	0	0	0	0	0

END ADC NO. 4 TEST, 0000 ERRORS

FIGURE 30-1 TSTAD4 DOUBLE-PRECISION HISTOGRAM

Documentation for this test will be supplied at a later time.
Software however is currently available.

Documentation for this test will be supplied at a later time.
Software however is currently available.

PROGRAM NAME TSTETU

TEST MNEMONIC TSTETU

PROGRAM FUNCTION This routine tests the performance of Event Timing Unit (ETU). Specifically, this test verifies the Reply/Reject responses, status and function commands, all three interrupt modes, and performs frequency measurements against an input standard frequency. TSTETU will test up to 8 cards simultaneously provided all cards are installed in the same 1750-1/2 module (do not have to be in contiguous slots) and they all share the same interrupt line. TSTETU is compatible for simultaneous multiple test operation.

OPERATING CONSTRUCTIONS Once TSTETU is given its initial control it will request parameters that control all remaining test execution and comments. The opening message is output as follows:

```
BEGIN @SE EVENT TIMING UNIT TEST
SHORT FORM OUTPUTS (1=NØ  2=YES)?
```

This question allows input to control whatever the parameter request messages are "short", abbreviations of the command, or "long", detailed description allowing execution parameter input without consulting the manual.

NOTE: Any input other than that requested will result in an error and repeat of the previous request. If these successive errors are made, the program will terminate. This restriction is in effect at all times.

ADDITIONAL NOTE: Even if short form message are selected, the operator may obtain the "long" version by entering 0 or simply a carriage return (CR). The program will respond with the longer version as long as a 0 or (CR) is input instead of real data.

Once the comment length mode is selected, the program offers the operator the option of using all the old parameters rather than having to input them again.

USE OLD CONFIGURATION(S) (1 = Yes 2 = No)?

A "1" input will skip to the TESTS, RUNS, PASSES step described later. The previously entered configuration and interrupt line definitions will be used.

If "OLD" parameters are not selected then input continues.

The next series of statements and parameter requests establish the equipment to be tested and the configuration of each card (long format output):

CONFIGURATION: W, T, S, (FFFF FOR DONE)

W = WEMS CODE (HEX)

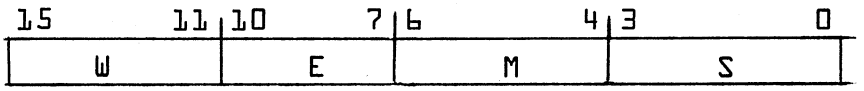
T = TIME UNIT VALUE (MICROSEC/COUNT) (1 to 127 DEC)

S = SAMPLE INTERVAL BY POWER OF 2 COUNTS (10 to 13 DEC)

#1? (FIELD 1), (FIELD 2), (FIELD 3) (CR)

At this point the operator should input the details as described below:

W = (Field 1) a two to four digit hexadecimal number equal to the 16-bit code to be loaded into the Q-register to address the given ETU.



W = Converter code and must always be 0

E = Equipment code of 1750-1 equipment (Even or odd number)

M = Module number that houses the ETU (after card #1 this value must be the same for all successive ETU's entered)

S = Slot number of the ETU within the module

This number may be a repeat of other entries but may not be zero.

T = (Field 2) The sample interval unit count as selected on the ETU card by its hardwire jumper options. This value is required for frequency and overflow calculations. The value T is usually in units of micro-seconds, but if a card is using an external irregular time base, then T should be approximated. (If no close approximations is possible set T=1 and perform calculations yourself).

S = (Field 3) A two digit decimal input (10 through 13) defining the bit number from the time counter that is used to enable the update of the registers. The bit jumpered sets the minimum sample interval for the event timer. This input is required to calculate the frequency required to cause an event overflow to occur

Each set of inputs must be terminated by a (CR) . If all these inputs are valid, then the program will respond with a next card request (up to 8). If an error is made, the program will request the same card number parameters. The operator may terminate input at any time by entering a negative hexadecimal number (such as FFFF) in place of the WEMS parameter.

After ETU parameter inputs are complete the program requests the interrupt line.

COMMON INT LINE NO. (2-15)?

The operator input should be a 1-2 digit decimal number for the interrupt line from 2 to 15. An unrelated response will cause a new request. If the interrupt line is already assigned to another program an error response is given and a new request made.

The final input request is for execution control parameters.

TESTS, RUNS, PASSES

TEST WORD=>BITS 1-6 = TEST TYPES

```
1 = RPLY/RJCT              2 = FUNCTION
3 = NORMAL INT             4 = EVENT OVFLW INT
5 = TIME OVFLW INT         6 = FREQUENCY

RUNS = NUMBER OF EXECUTIONS (8000 = INFINITE)

PASSES = NO. OF TIMES TO EXECUTE SINGLE TESTS
? (Field 1), (Field 2), (Field 3)
```

The program expects an input for each of the three fields. Any unrelated entry will be counted as an input error and a new request will be made.

TESTS = (Field 1) This word is a 1-2 digit hexadecimal number corresponding to the test control word. Most of the bits are defined individually and described in the comment statements above. The TESTS word may not be zero or else an input error is counted and a new request made.

Any test bit equal to a 1 will cause execution of the corresponding test reaction. Setting any other unassigned bit will not cause any test execution.

RUNS = (Field 2) A 1-4 digit hexadecimal number specifying the runs through all selected tests. If RUNS = 8000 then the diagnostic will execute until directed to stop. RUNS may not be zero.

PASSES = (Field 3) A 1-4 digit hexadecimal number to specify the number of times to execute each individual test before continuing on to the next selected test. If PASSES = 8000 then the diagnostic will execute the first selected test until directed to stop. PASSES may not be zero

After all tests are run and all sections repeated the test will output a termination message.

```
END TSTSTU  TESTS=TTTT  RUNS=RRRR  ERRORS=EEEE
```

The three output values in the termination message detail the state of execution when the test finished or was directed to stop.

TTTT = a 4-digit hexadecimal repeat of the input parameter TESTS

RRRR = the present run count at termination. If the test executed undisturbed until termination then this should equal the input RUNS parameter.

EEEE = an accumulated error count of all errors. Each test may have more than one error counted per pass if they are separate error types.

There is no indication of the current pass count, so if a parameter exit is directed then even if the program has run 50 passes of all tests but the last and haven't completed the last test loop yet, RUNS will still be zero.

During test execution any error detected will be noted and an error message printed (if enabled) after the test section terminates. Each individual test has its own encoded error word with bits assigned to the error word to specify each failure. In addition, the card number as input is given to pinpoint the failure

```
#i   ERR0R=code    W=wems
```

For test 3, 4, and 5, this line is followed by the data status input from the card

```
DATA=dddd          STAT=ssss
```

i = a number from 1 to 8 corresponding to the input parameter set.

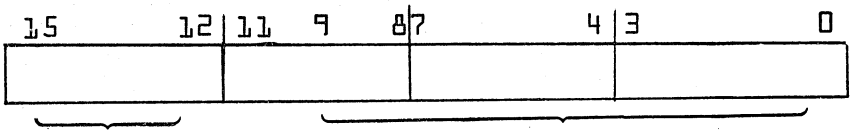
code = a 4-digit hexadecimal error code word, the first (high-order) digit of which is the test section number (see code details below).

wems = the input wems code used to address the failed card.

dddd = the 4 digit hexadecimal value received from a data input (this may be all zero if a reject or time-out fault is detected.

ssss = the 4-digit hexadecimal value received from a status input (may be all zero as above).

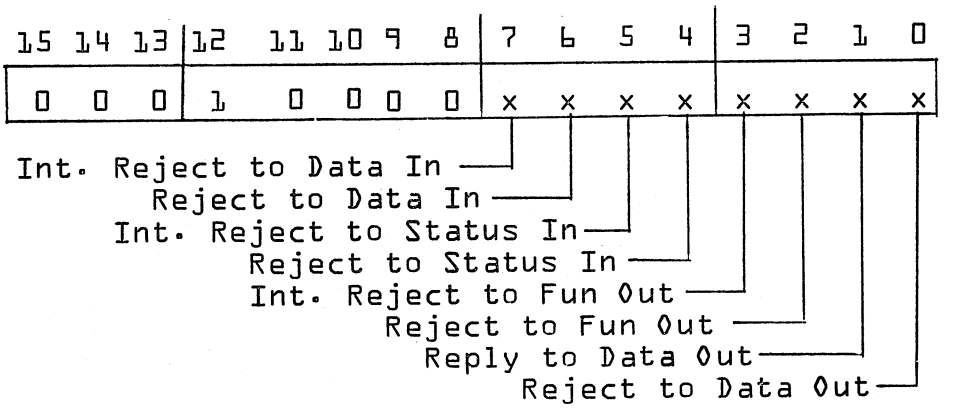
The error code word is further described as follows: {The error status is given as the error detected, i.e., "event overflow" means one was detected when not expected}:



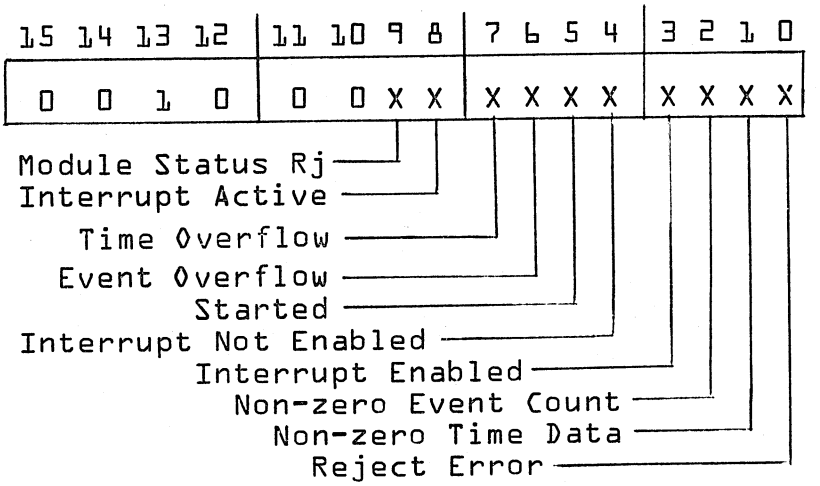
test section number

individual errors set by bit for each test failed

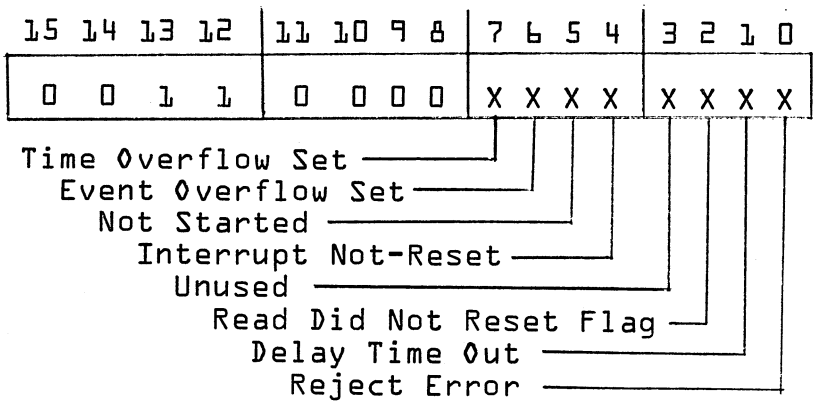
for Test 1 {Reply/Reject}



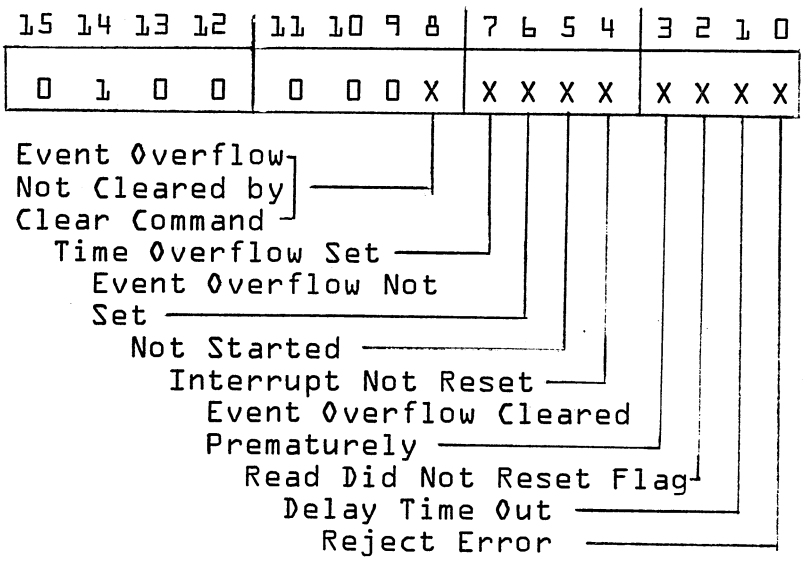
for Test 2 {Function/Status}



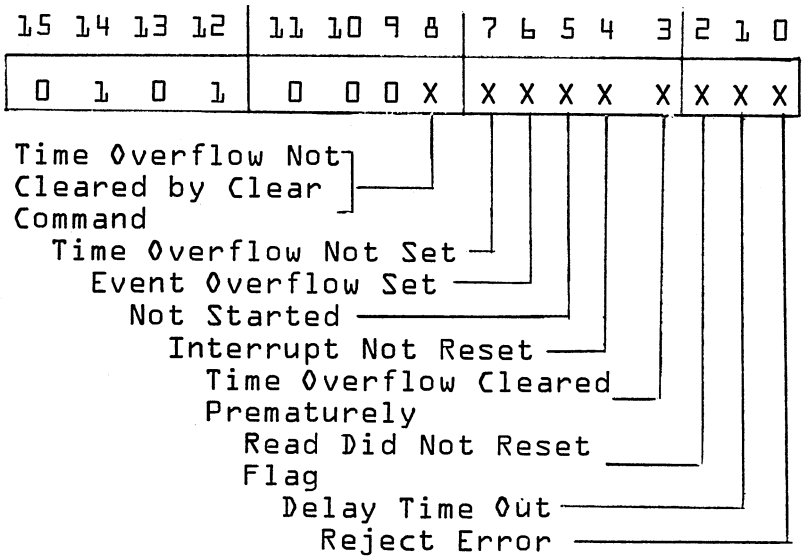
for Test 3 {Normal Interrupt}



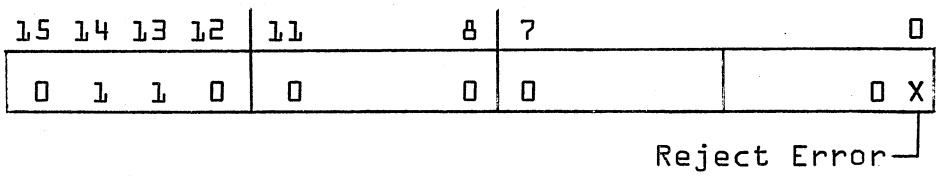
for Test 4 {Event Overflow Interrupt}



for Test 5 {Time Overflow Interrupt



for Test 6 (Frequency Calculation)



PROGRAM DESCRIPTION

The data entry section of the program, described in detail above, interfaces to the operator and executes at execution priority level 4 as does the bulk of the test portion of TSTETU. During interrupt testing there is a software "time-out" delay loop in the program which is scheduled to execute at Level 1. This allows operation of other programs simultaneously but insures that eventually TSTETU will detect any interrupt failure at the time-out and reschedule itself at Level 4 to process the failure and continue the test.

The input common interrupt line is selected at level zero until such time that interrupt testing is begun. At this time the interrupt line priority processor is increased to level 11 for rapid, but not absolute, interrupt response.

Execution begins with Test 1, if selected, and steps from card 1 through all selected cards, loops in this first test "PASS" number of times, and then proceeds on to the next sequentially selected test. Each test will ask for its specific input parameter or stimulation state only on the first pass through the test requiring that the user not make multiple RUNS (loop on all tests) with incompatible tests such as event and time overflows (since one requires exceptionally slow, one exceptionally fast event inputs).

Test 1 Reply/Reject. A test verifying the card's reply/reject logic The test performs the following I/O commands and expects the corresponding response:

Data Input	⟶	Reply
Data Output	⟶	Internal Reject
Status Input	⟶	Reply
Function Output	⟶	Reply

Test 2 Function/Status. Verify the steady-state signal levels and function command state manipulation. This section executes the following function commands and expects the corresponding data/status state to be present {no events must be present}:

Step	FUNCTION	TIME COUNT {HEX}	EVENT COUNT {HEX}	NOT STARTED	INTERRUPT ENABLE	INT FLAG	EO	TO
1	Clear Card	0000	000	ON	OFF	OFF	OFF	OFF
2	Set Interrupt Enable	0000	000	ON	ON	OFF	OFF	OFF
3	Clear Interrupt Enable	0000	000	ON	OFF	OFF	OFF	OFF
4	Set Interrupt Enable	0000	000	ON	ON	OFF	OFF	OFF
5	Clear Card	0000	000	ON	OFF	OFF	OFF	OFF

Test 3 Normal Interrupt. Execution of this test section requires that all cards under test be connected to the same interrupt line and that each has an event rate input within the measurable range {i.e., not so fast as to cause Event Overflow and not so slow to cause time overflow}. This range is output to the operator per card on the first pass and execution does not begin until the operator sets the frequency and signals "go ahead". The output message is as follows:

#c SET 11.11 HZ < f < hhhh KHZ?

c = Card number corresponding to entry order
11.11 = Low range value for input frequency f {decimal}
hhhh = High range value for input frequency f {decimal}

The go-ahead input must be a (CR) .

The ranges are calculated using the characteristic input parameters per card.

11.11 = 1/Maximum Time Interval

Max Time = {2**16 counts} * {T usec/count}
= 65536 * T * {10** {-6} sec}

11.11 = 1/(65536 * T (E-6))
=(10**6)/(65536*T) = (appx.) 1526/T sec

11.11 = (15.26/T) Hz

hhhh = Maximum count/Total sample interval
= (2**12)/(2**S) *T(E-6) sec (S=10,11,12,13)
= (2**2)/2**(S-10) *T(E-6) sec
= 4000/2**(S-10) *T KHZ ///

Once the calculations are made and output, the frequency is adjusted by the operator, and a CR is input, then test execution begins. The interrupt line response priority is raised to level eleven from zero. The card is cleared, the interrupt enabled, and a delay routine scheduled at level one is entered. Hopefully an interrupt causes exit from the delay routine before its termination. A check is made to verify no overflows, that a read clears the interrupt, that the Not Started status goes away, and that a clear then resets Interrupt Enable before exiting the test section.

Test 4 Event Overflow Interrupt. The value calculated for the high limit f in Test 2 is used to specify an Event Overflow causing input to the operator. Again a (CR) is the go-ahead signal:

#c SET f > hhhh KHZ (KEY)?

The delay routine is entered while the program waits for an Event Overflow interrupt. Once the interrupt is received, a check is made to verify Event Overflow and no Time Overflow, a read clears the interrupt, that the Not Started status goes away, and that only a clear command clears Event Overflow.

Test 5 Time Overflow Interrupt. Like the Event Overflow test, this test uses one of the calculated frequency limit values as an input specification. The low end value is requested to insure a start event but no following update event before the time count elapses.

#c f < 11.11 HZ (KEY)?

Once a time overflow interrupt is received while in the delay routine the same checks as in Test 4 are made to verify the overflow and card operation.

Test 6 Frequency. This test may be used as a tool to verify the accuracy of the ETU card if a known frequency source is available. Additionally, this may be simply used as a

diagnostic monitoring routine to monitor and output frequency rates and changes.

The frequency test is completely status driven and so it may be used to test cards in system configurations not using the interrupt capabilities. Each pass through the test performs a data and status input, calculates the resulting frequency scaling the result to correspond to the card's selected unit interval (T), and outputs the result as it changes. A simple input:

RANGE = ? rrrr

is requested on initial entry and is used by the program to control its calculated frequency outputs. The output calculated frequency value is a 5-digit decimal number with an attenuation factor from 1 to 10^{-3} (such as, 12345 @ -2 = 123.45). If this calculated frequency compared to the previous reading's calculation is within plus or minus the Range, with equal attenuation, then the frequency is not output. Any measurement in excess of the Range or with a different attenuation factor will be printed. In addition, if either overflow indicates, or not started are indicated then the resulting data/status inputs will be output.

#c TSTETU W = wems T = dddd E = seee F = fffff @ -a

c = Card number corresponding to the input order
wems = Input card WEMS code
dddd = The 16-bit hexadecimal data received from the card from a data input (equals time count)
seee = The 16-bit hexadecimal event and status data input via a status input. The low order 12 bits correspond to the event count, the high order 4 bits the status.
fffff @ -a = The 5-digit decimal value and single-digit decimal attenuation calculated frequency value. The range of fffff is from 1 to 32767 and of 'a' is from 0 to 3. By example them, 12345 @ -2 is equal to the frequency 123.45 Hz.

The only error detection processing in Test 6 is of Rejects. Any time either an internal or external reject is encountered the program will output an error message and terminate the pass.

PROGRAM NAME: CRTCTU

TEST MNEMONIC: TSTCTU

PROGRAM FUNCTION:

This routine tests the performance of the 1595-1X Serial Input/Output Unit in conjunction with the FACIT 4203/0006 Cassette Tape Unit.

The test is divided into three sections:

1. Write Patterns test
2. Read patterns test
3. Read records test

All possible error conditions are monitored and a message is output for each error condition detected.

The 1595-1X must be mounted in a 1750-1 Computer Interface Unit or a 1750-2 Computer Interface Expander connected directly to a 1750-1. The unit must have the appropriate jumpers and cable to the FACIT 4203.

The interrupt line for the 1595-1X must be connected to the CPU.

OPERATING INSTRUCTIONS:

Once TSTCTU is in control, a message is output on the Standard Output Comment Medium {SOCM} as follows:

BEGIN 4203 FACIT CASSETTE TAPE TEST
TESTS, RECORDS, RUNS

NOTE: At this time the operator should insure that the test cassette has been installed in the cassette tape unit.

The program then enables the Standard Input Comment Medium {SICM} for user keyboard input of three control parameters in the following format:

{Field 1}, {Field 2}, {Filed 3} (CR) where:

OPERATING INSTRUCTIONS (Cont'd.):

Field 1 — 1 to 4 hexadecimal digits representing 16 bits with the following assignments

Bit 1 = "1" do Test 1
Bit 2 = "2" do Test 2
Bit 3 = "3" do Test 3

Field 2 — 1 to 4 hexadecimal digits representing the number of records to be done in each of the specified tests. If the number exceeds $3E8_{16}$, the program will repeat request of these parameters.

Field 3 — 1 to 4 hexadecimal digits specifying the number of times the test sequences are to be done. If bit 15 is set the test will execute until halted by user.

Next, a message is output on the SOCM as follows:

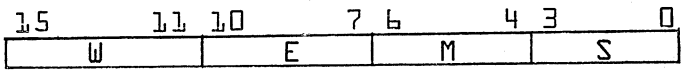
1595 INT LINE, WEMS CODE

Accordingly, the user must enter two control parameters on the SICM in the following format:

(Field 1), (Field 2) CR where:

Field 1 — the decimal interrupt line number for the 1595-X card, it must be in the range of 2 to 15.

Field 2 — 1 to 4 hexadecimal digits representing the 16 bits that are loaded into the "Q" register to address the 1595-X (SIO)



where W = converter code which is normally zero.
E = equipment number of the computer interface unit.
M = module number of the unit holding the SIO.
S = station number of the SIO within the module.

OPERATING INSTRUCTIONS (Cont'd.):

The interrupt line input is checked for correct range and whether that line is currently busy. If the line number is not in range or is currently busy, the following message is output on the SICM:

TSTCTU INTERRUPT ASSIGNMENT ERROR

The parameters are requested again, if this error is repeated three times in succession, the test is terminated.

Upon completion of the number of repeats of the test sequence requested or when halted by user, the program outputs a message on the SOCM as follows:

END CASSETTE TEST hhhh RUNS hhhh ERRORS

where hhhh is some hexidecimal number.

The program then clears the flay word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION:

When error conditions are detected, a message is output to describe the error condition.

Data errors are described with the following input:

RECORD hhhh DATA ERROR, WORD hhhh ACTUAL hhhh EXPECTED hhhh

where hhhh is a hexidecimal number, the record is numbered from the beginning of the tape and the word is numbered from the beginning of the record.

Driver detected errors cause an output message in the following format:

RECORD hhhh RQ=hh CODE=hh SI=hhhh SC=hhhh SE=hhhh

where: h is a hexidecimal digit
RQ = monitor request code
CODE = alternate device error code
SI = equipment status at initial entry to driver
SC = equipment status at continuator entry to driver
SE = time out status

NOTE: The upper eight bits of the status are the status bits of the 1595-X and the lower eight bits are the status bits of the cassette tape unit.

ERROR MESSAGE DESCRIPTION (Cont'd.):

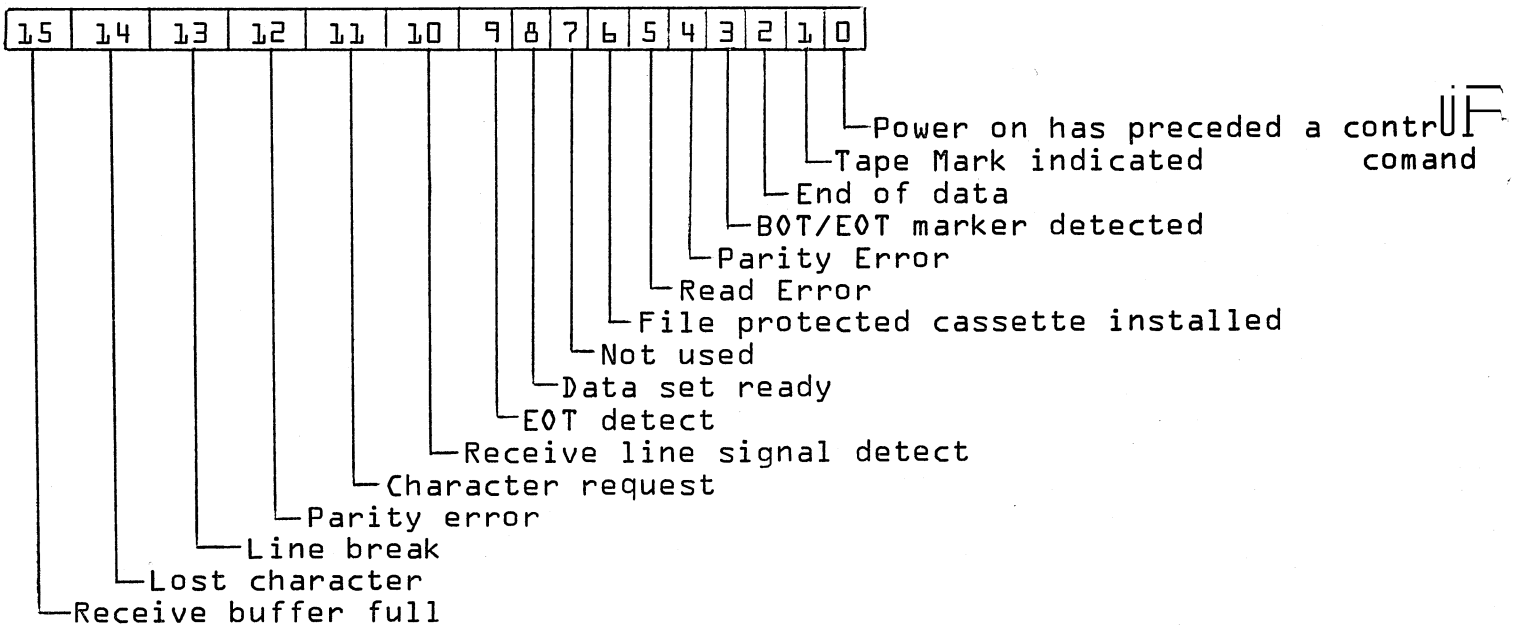
Monitor Request Codes:

04 = Read request
06 = Write request
14 = Rewind request

Driver alternate device error codes:

00 = Time out error
01 = Lost data
03 = Read error
04 = Checksum error
05 = Internal reject
06 = External reject
10 = Non-negative record length
13 = File protection
14 = Not ready
33 = Line break
60 = No character received when expected

The status bits are defined as follows:



PROGRAM DESCRIPTION:

Before the test sequence can be conducted, the user must input the control parameters and the test configuration. Upon completion of these inputs each of the specified test sections is conducted in sequence.

PROGRAM DESCRIPTION (Cont'd.):

Each test section will run the specified number of records unless stopped by the operator or by a condition which will not allow it to continue.

The specific structure of each test is as follows:

Test Section One - This is a write patterns test. The cassette is issued a Rewind and Advance to Beginning of Tape command. Following completion of the Rewind command, the specified number of records are written on the tape using the following patterns of hexidecimal digits: 00, 11, 22, 33, 44, 55, 66, 77, 88, 99, AA, BB, CC, DD, EE, and FF. Each record contains only one set of digits repeated through the record. This test section will terminate on line break, file protection or end of tape.

Test Section Two - This is a read patterns test. The cassette unit is issued a Rewind command. Upon completion of the Rewind operation, the specified number of records are read and the data is compared to the data that was written in Test Section One. Any difference in data causes a Data Error message to be printed. This test section will terminate on line break, end of data or end of tape.

Test Section Three - This test section reads, records and prints out errors detected by the driver. It can be used to verify that data on cassette has been written in the format expected by the driver. The specified number of records are read unless terminated by detection of a line break, end of data, or end of tape.

PROGRAM NAME — CRMOLY

TEST MNEMONIC — RTOLY

PROGRAM FUNCTION — This routine provides the user with a conversational means of exercising the hardware within the system. The hardware is exercised in discrete steps as defined by the operator. The steps are defined within the OLYMPUS statement{s} as explained in the following paragraphs.

OPERATING INSTRUCTIONS — Once RTOLY is in control, a message is output on the Standard Output Comment Medium {SOCM} as follows:

```
BEGIN REAL-TIME OLYMPUS
FWA = XXXX
NEXT
```

where XXXX is a hexidecimal number indicating the starting point of RTOLY.

The program then enables the Standard Input Comment Medium {SICM} for user input of a valid "OLYMPUS" {RTOLY} statement in the following format:

MNE, Field 1, Field 2, - - - - - - - Field 8 CR

where MNE is a mnemonic of up to four characters followed by a maximum of eight fields. Each field can have a maximum of four digits. The statement is terminated by a carriage return.

Once the carriage return (CR) is entered, the mnemonic is decoded and a search is made to determine the address of the processor for that menemonic. If no processor can be found the message:

MNEMONIC NOT FOUND

is output on the comment device and the user must enter another statement.

When the processor is located, the fields are decoded and loaded into the value table. The fields are checked for correct format, illegal characters and/or more than eight fields.

The following are error messages which may be output during field decoding:

ILLEGAL CHARACTER - A character other than 0 through 9 or A through F was found while decoding field.

FORMAT ERROR - Indicates an error in use of parenthesis or a hexidecimal character was input with labeled storage.

MORE THAN 8 FIELDS - The eighth field was not terminated by a carriage return.

ILLEGAL FIELD - Mnemonic or field terminated by an asterisk or period. Statement number in indirect mode not terminated by space.

Each of the above errors will cause processing to terminate. The user must enter a new statement.

Following decode of fields control is transferred to statement processor. If an error occurs during the processing of a statement, the following message is output if the processor takes the error exit:

PROCESSOR ERROR EXIT

The user can then enter another statement.

When processor execution is complete, the user is requested to enter another statement.

STATEMENT FIELDS

The statement fields an "OLYMPUS" processor will recognize and accept are as follows:

1. Hexidecimal numbers

   All values are entered as hexidecimal numbers. A field is normally four or less digits in length without sign. If more digits are entered, only the last four will be used. This feature can be used to correct field errors without deleting the whole statement, as long as only hexidecimal values are involved in the error.

2. Labeled Storage

A table of 20 memory locations within "CRMOLY" are provided for storage and are addressable with the alphabetic characters "G" through "Z".

3. Parenthesis

Parenthesis, in conjunction with hexidecimal values or labeled storage, are used as a means of indirectly addressing memory. Two levels of indirect addressing are available for hexidecimal values. One level is available for labeled storage locations (because labeled storage itself already implies one level of indirect addressing).

The following table defines the five possible combinations that are provided for specifying quantities. "HHHH" is a hexidecimal number and "LS" is one of the labelled storage locations.

Field	Operand
HHHH	Hexidecimal member
(HHHH)	Contents of address specified by HHHH
((HHHH))	Contents of the address which is specified by the contents of the address specified by HHHH.
LS	Contents of the address associated with the specified labelled storage.
(LS)	Contents of the address which is specified by the contents of the address associated with the specified labelled storage.

NOTE: In "OLYMPUS" statements with field parameters designated by "Hi", specifying the parameter as "HHHH" has no meaning when that field defines a location into which data is to be stored. "HHHH" is interpreted as a hexidecimal member and not a memory location. Any of the other four formats are meaningful. When the hexidecimal number is to imply a memory location the parameter will be defined as "memory location".

MODES OF OPERATION

CRMOLY has two modes of operation. The direct mode is used when the operator wishes to compose, enter and execute each statement separately. In the direct mode an attempt is made to execute the statement as soon as entry is complete. The indirect mode allows a series of statements to be entered, editted, stored and then executed in sequence when directed by the operator.

INDIRECT MODE OF OPERATION

The direct command:

INPT (CR)

signals CRMOLY that a program sequence is to be defined. Before a sequence is defined, any previous sequence is cleared. OLYMPUS commands are then accepted in any order but each command must be preceded by a statement number which defines the location within the program sequence.

The statement number has the following format:

M.N

where: M is a decimal number with a range of 1 to 320. N is a decimal number with a range of 0 to 99. The decimal point must be specified, but N may be omitted.

The statements may be entered in any order, but priority of execution follows ascending order of value of statement number. The decimal point is a separator rather than a true decimal point, as shown in the following sequences:

1.
1.1
1.2
1.10
1.11
1.90
1.99
2.0

A space is required to terminate the statement number before the mnemonic and field portion are begun. The format of the statement is therefore:

M.N MNE, field 1, field 2, - - - - field 8 (CR)

When the carriage return is entered the statement is checked for correct format. All error messages that apply in direct mode also apply in indirect mode. When an error is detected, the statement is deleted. When the statement number is the same as one previously entered, the earlier statement is replaced by the new one. When the statement is verified and threaded into sequence the user is requested to enter next statement. Statement definition continues until:

END (CR)

is entered. The message is then output:

STATEMENT DEFINITION COMPLETE

To exit program sequence at any point, the following statement must be entered in the program sequence:

M.N EXIT (CR)

The program sequence is automatically terminated when the highest statement number is encountered.

To delete a statement, the following is entered.

M.N CLSN (CR)

Where: M.N must equal a previously entered statement number or an error will occur indicated by the following message:

STATEMENT NUMBER NOT FOUND

The statement is ignored.

The program sequence can be edited to modify existing statements or add new ones by entering the direct command.

EDIT (CR)

The input of statements following the EDIT command is the same as when following the INPT command. However, the previously entered program sequence is not cleared.

The program sequence that has been entered can be examined by the direct command:

LIST, M.N, M. N (CR)

where: M.N indicates the beginning and ending statement numbers to be listed. If the first statement number is not entered, the complete program is listed. If the second statement number is not entered, the program is listed from the first statement number specified through the end. If there are no statement numbers equal to the statement numbers input, listing will start at the first statement number greater than that specified and end with the last statement number that is lower than that specified.

To begin execution of program sequence, the following direct command must be entered:

EXEC, M.N (CR)

where: M.N indicates the first statement number to be executed. If the statement number is not entered or can not be found, execution starts at lowest statement number.

The following statements are illegal if requested in the indirect mode:

LST, LHX, DEV, INPT, EDIT, LIST, EXEC

The following statements are illegal if requested in the direct mode:

MSG, INT, IFSK, IFGT, IFLT, IFEQ, IFNE, GOTO, END, CLSN, PAUS

CORE RESIDENT REAL TIME OLYMPUS STATEMENTS

Real Time OLYMPUS (RTOLY) statements fall into roughly four categories and are grouped accordingly in the following statement definitions.

The four categories are: (1) Operator Interface Statements, (2) Program Control Statements, (3) Arithmetic and Logic Statements, and (4) Hardware Interface Statements.

OPERATOR INTERFACE STATEMENTS

Operator interface statements are those which allow the user to define, control, start, stop or otherwise direct the execution of his program sequence.

LST CR (Direct mode only)

List available OLYMPUS or RTOLY statement set. Each mnemonic that can be used is listed followed by the absolute address of the processing routine.

DEV, XXX (CR) {Direct mode only}

Output device is as specified for all mnemonic processing routines which call PRINT subroutine, such as: LIST, LST, MSG. Two devices can be specified; TTY for teletype or SOCM, and LST for standard list device which would be line printer if driver is loaded. If XXX equals other than TTY or LST, it is an error and no change occurs.

INPT, EDIT, LIST, EXEC, END, CLSN

These mnemonics have been previously defined.

DEFN, LS, LS, ------ CR

Define labeled storage - this statement permits the user to define the contents of labeled storage in a conversational mode. On execution of this statement, RTOLY outputs on the comment device "LS=". The user must then enter the value to be stored in the labeled storage specified.

Example: DEFN, G, H (CR)
G = 1234 (CR)
H = 5678 (CR)

Indirect addressing {parenthesis} are not permitted.

TYPE, LS, LS, - - - - - (CR)

Output Labeled Storage Values - This statement permits the contents of labeled storage to be output on the list device.

Example: G=1234 H=5678

Up to eight values can be output from each statement. Indirect addressing {parenthesis} are not permitted.

MSG, message (CR) {Indirect mode only}

Output message - this statement allows user to output messages on the list device. The comment begins immediately following the mnemonic terminator comma, and may be up to 60 characters in length. Execution of statement causes message to be output.

EXIT (CR) {Indirect mode}

Exit indirect mode - This statement when encountered returns control to direct mode.

EXIT (CR) {Direct mode}

Exit direct mode - This statement ends execution of RTOLY in direct mode. If an indirect program sequence has been entered, it will be saved and RTOLY must be restarted by "RESUME, RTOLY" command.

OFF (CR) {Direct mode only}

End RTOLY - This statement ends execution of RTOLY in direct or indirect mode. If an indirect program sequence has been entered, it will be cleared and memory released. To restart RTOLY enter "START, RTOLY" command.

PROGRAM CONTROL STATEMENTS

Program control statements are those statements which are used to control and/or direct execution of the program sequence while the program is executing in the indirect mode.

STOR, H1, H2 (CR)

Store Value - The value specified by H1 is stored at the address specified by H2.

IFGT, H1, H2, M.N (CR) {Indirect mode only}

Logical "If Greater Than" - If H1 is greater in value than H2, go to statement number specified by M.N; if not, go to next higher statement number.

NOTE: In all "IF" statements +0 {0000} is equal to -0 {FFFF}.

IFEQ, H1, H2, M.N (CR) {Indirect mode only}

Logical "If Equal" - If H1 is equal in value to H2, go to statement number specified by M.N; if not, go to next higher statement number.

IFLT, H1, H2, M.M (CR) {Indirect mode only}

Logical "If Less Than" - If H1 is less than H2 in value, go to statement number specified by M.N; if not, go to next higher statement number.

IFNE, H1, H2, M.N (CR) {Indirect mode only}

Logical "If Not Equal" - If H1 is not equal in value to H2, go to statement number specified by M.N; if equal, go to next higher statement number.

IFSK, M.N (CR) {Indirect mode only}

If skip switch set - If selective skip switch is set go to statement number specified by M.N; if selective skip switch is not set, go to next higher statement number.

GOTO, M.N (CR) {Indirect mode only}

Transfer control - Go to statement number specified by M.N.

PAUS, H (CR) {Indirect mode only}

Type H and pause - This statement outputs the message "PAUS HHHH" and waits for user to input carriage return.

DELY, H (CR) {Indirect mode only}

Delay - This statement causes a delay of H times 100 microseconds to occur while in this statement processor. The time required to access this statement processor {about 200-microseconds} is not included.

INT, H1, H2, H3, H4, M.N (CR) {Indirect mode only}

Interrupt handling - This statement allows for an interrupt from peripheral equipment to be handled. The interrupt line is enabled. The routine waits until an interrupt is received or the time delay specified has expired. In either case, the interrupt line is released. If no interrupt is received, control is transferred to statement specified in last parameter. If specified, a message will be output indicating an interrupt was received, "INT LING XX", where XX is from 02 to 15 decimal.

H1 = interrupt line in hexadecimal, must be in range of 2 to F.

H2 = wait time in multiples of 100 microseconds must be a positive number.

H3 = memory location where number of interrupting line (2-F) is to be stored.

H4 = if zero, store line number only, if non-zero output line number message also.

M.N = statement number to which control is transferred if no interrupt occurs.

ARITHMETIC AND LOGIC STATEMENTS

Arithmetic and Logic statements perform specified arithmetic or logic functions as defined by the statement.

ADD, H1, H2, H3 (CR)

Addition - the value specified by H1 is added to the value specified by H2. The sum is stored at the address specified by H3.

NOTE: In this and in the following tables, Hi may refer to a hexidecimal number, a labeled storage location, or an indirect address. If Hi is used to specify a cell into which a value is to store, it may not be a hexidecimal number. (See description on statement fields).

SUB, H1 H2, H3 (CR)

Subtraction - H2 is subtracted from H1 and the result is stored at H3.

MUI, H1, H2, H3 (CR)

Multiply - H1 multiplied by H2 is stored at H3.

DVI, H1, H2, H3 (CR)

Divide - H1 is divided by H2 and the result is stored at H3.

EOR, H1, H2, H3 (CR)

Exclusive OR - the "Exclusive OR" comparison of H1 and H2 is stored at H3. This is a bit by bit comparison of H1 and H2. The corresponding bit in the resultant is set only if the bit in H1 or the bit in H2 is set. The bit in the resultant will not be set if the bit in H1 and the bit in H2 are both set.

AND, H1, H2, H3 (CR)

AND (logical product) - The "AND" comparison of H1 and H2 is stored at H3. This is a bit-by-bit comparison of H1 and H2. The corresponding bit in the resultant will be set only if the bit in H1 and the bit in H2 are both set.

OR, H1, H2, H3 (CR)

Inclusive OR - The "Inclusive OR" comparison of H1 and H2 is stored at H3. This is a bit-by-bit comparison of H1 and H2. The corresponding bit in the resultant will be set if the bit in H1 or the bit in H2 is set, or if both bits are set.

RSFT, H1, H2, H3 (CR)

Right Shift Data - The value specified by H1 is right shifted the number of bits specified by H2. H2 must be in the range of 0 to F hexidecimal. The resultant value is stored at the address specified by H3. Right shift causes the sign bit to be extended.

LSFT, H1, H2, H3 (CR)

Left Shift Data - The value specified by H1 is left shifted the number of bits specified by H2. H2 must be in the range of 0 to F hexidecimal. The resultant value is stored at the address specified by H3. Left shift is an end around operation.

HARDWARE INTERFACE STATEMENTS

READ, H1, H2, H3, H4, H5 (CR)

Execute input command - This instruction causes one or two input instructions to be executed.

H1 = contents of Q register on second input if H3 is entered or first input if H3 is not entered or equals FFFF.

H2 = address to store data input from address specified in H1.

H3 = contents of Q register on first input. Input is not executed if H3 equals FFFF.

H4 = address to store reject code

H5 = non-zero, the data input (H2) will be output as message "A=xxxx".

The first input to be executed is specified by H3 to connect (old type 1500 equipments) if parameter is entered and not equal to FFFF. The second input specified by H1 to continue (old 1500 channel address). Data input from H1 will be stored at H2. If H4 is entered, the reject status is stored at address specified by H4 and is defined as follows:

Reject code = 0 = no reject
Reject code = 1 = reject with H1 address
Reject code = 2 = reject with H3 address

Parameters H1 and H2 must always be entered. Parameters H3, H4 and H5 are optional

RITE, H1, H2, H3, H4 (CR)

Execute output command - This statement causes an output instruction to be executed following an optional input instruction.

H1 = contents of Q register for output instruction
H2 = data to be loaded into A register for output
H3 = contents of Q register for input instruction. Input is not executed if parameter is not entered or is equal to FFFF.
H4 = address to store reject code

The input instruction is executed first if specified by H3 to connect (old type 1500 equipments). The output instruction specified by H1 is executed to continue (old 1500 channel address). H2 specifies the value to be output. If H4 is entered, the reject status is stored at address specified by H4 and is defined as in "READ" command.

Parameters H1 and H2 must always be entered. Parameters H3 and H4 are optional.

RJTP, H (CR)

Specify reject option - Internal and external rejects may be handled by a common routine. This routine prints a comment containing information about the reject. This command allows user control of the comment printout by specifying H. Where H may have one of the following values:

H = zero, printout is bypassed.
H = N, printout is discontinued after N number of printouts if not re-initialized by this statement.
H = 8000, printout always occurs.

ENTR, memory address, H2, H3 . . . . H8 (CR)

Enter data - This statement allows the entry of seven values in sequential storage locations defined by memory address. This value does not require parenthesis. H2 through H8 are the seven values to be stored.

This statement should be used with caution as the user must avoid entering data in memory locations that are in use.

Documentation for this test will be supplied at a later time.
Software however is currently available.

PROGRAM NAME CRTCCD

CDD 2- SCSI

MNEMONIC NAME TSTCCD

PROGRAM FUNCTION

The 1833-4/1866-1X Test Routine is a series of test designed to exercise and determine the performance of the 1833-4 Cartridge Disk Drive Controller and the 1866-12 or 1866-14 Cartridge Disk Drives in their various modes of operation using the MSOS driver. The user must specify the dimensions of the disk section to be tested and the particular operations to be performed as part of the test sequence. The program exercises and monitors the performance of the following operations:

1. Read/Write head switching.
2. Core-to-disk transfers of information ① in block lengths 2048_{10} words.
3. Disk-to-core transfers of information ① in block lengths 2048_{10} words.
4. Transfer of information from a specified core/disk location to a specified disk/core location.
5. Read head positioning (seek operation).

Any errors sensed during the conduct of a test will cause appropriate diagnostics to be output on the Standard List Device (SLD). The program will diagnose any of the following discrepancies:

1. Alteration of information during core-to-disk or disk-to-core transfers.
2. Transferred information displaced from destination locations.

---

① Information includes four worst patterns ($9555, $6AAA, $5A5A and $A5A5), all ones, and pseudorandom bit patterns.

3. Lost data, address, seek, defective track and storage parity errors during write operation.

4. Lost data, address, seek, protect fault, defective track, check word and storage parity errors during read operation.

OPERATING INSTRUCTIONS

Once TSTCCD is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

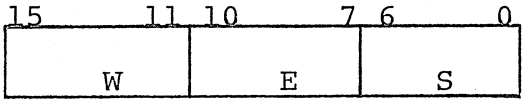
BEGIN 1833-4/1866-1X MULTIPLE CARTRIDGE DISK DRIVE TEST 1833-4 INT LINE/WES CODE

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of two control words in the following format:

(Field 1),(Field 2) (CR)

Where: Field 1 the decimal interrupt line number for the 1833-4 controller, must be in the range of 2 to 15.

Field 2 1 to 4 hexadecimal digits representing the 16 bits loaded into the "Q" register to address the 1833-4 controller as shown below:



Where: W = converter code which must be zero.

E = equipment number of the 1833-4 controller

S = station address - set to one by test routine.

The interrupt line input is checked for correct range and if currently busy (in use). If the line number is not in range or is currently busy, the following message is output on the SOCM:

TSTCCD INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again, if th

error is repeated three times in succession, the test is terminated.

Following the correct input of the interrupt line number, the following message is output on the SOCM:

UNITS TO BE TESTED

Accordingly, the user must enter one control parameter on the SICM in the following format:

(Field) (CR)

Where Field 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 0 = "1" Test Unit 0

Bit 1 = "1" Test Unit 1

Bit 2 = "1" Test Unit 2

Bit 3 = "1" Test Unit 3

The remaining bits are not used.

At least one bit must be set or the parameter is requested again.

If more than one bit was set, indicating that more than one unit will be tested, the follwing message will be output on the SOCM:

ARE PARAMETERS FOR ALL UNITS THE SAME?

Accordingly the user must enter one of the following via the keyboard of the SICM:

YES (CR) or NO (CR)

If YES is entered, the parameters for all units will be the same and the parameters will only be requested once. If NO is entered, the parameters will be requested for each unit to bettested.

Next the user will be requested to input the test parameters. The following message will be output on the SOCM:

PARAMETERS FOR UNIT a
TYPE, TESTS, BEG SEC, FND SEC, RUNS

Where a = 0, 1, 2 or 3 depending on the units to be tested. If YES was entered above "a" will equal ALL

The SICM will then be enabled for user keyboard input of five control words in the following format:

(Field 1),(Field 2),(Field 3),(Field 4),
(Field 5) (CR)

Where: Field 1 one digits as follows

zero fo 1866-12 single density disk, maximum sector address $5BFB, first sector or fixed disk is $2DFE

nonzeroffor 1866-14 double density disk, maximum sector address $B7F2, first sector on fixed disk is $5BFC.

Field 2 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 1 = "1" Do Test 1

Bit 2 = "1" Do Test 2

Bit 3 = "1" Do Test 3

Bit 4 = "1" Do Test 4

Bit 5 = "1" Do Test 5

Bit 6 = "1" Do Test 6

The remaining bits are not assigned.

Field 3 1 to 4 hexadecimal digits representing the disk sector address at the beginning of test area.

Field 4 1 to 4 hexadecimal digits representing the disk sector address at the end of test area.

Field 5 1 to 4 hexadecimal digits representing number of times the test sequence is to be run. If bit 15 is set, the test will execute until halted by the user.

If the beginning disk address is larger than the ending disk address or the ending disk address exceeds the size of the disk, the message below is output on the SOCM and the parameters are requested again.

TSTCDD SEC ADD ERR

Following acceptable input of test parameters the test sequence willbbegin.

Each unit to be tested will output the following message on the SOCM:

TSTCCD UNT a BEGIN

Where a = 0, 1, 2, or 3

When the test ends for a particular unit the following message is output on the SOCM:

TSTCDD UNT a END,hhhh RUNS,hhhh ERRORS

Where hhhh is some hexadecimal number.

When all units have completed, the following message is output on SOCM:

END 1833-4/1866-1X TEST

The program then clears the flag word and exists to the dispatcher.

ERROR MESSAGE DESCRIPTION

All error messages output by the program are output on the Standard List Device (SLD) and are of the same general format.

TSTCCD UNT d TEST (1) RUN (2)(3)(4) XFER H/W ADDR (5)

Where: a 0,1,2 or 3

(1) Decimal number of the test currently being executed.

(2) Hexadecimal number of the current pass three the test sequence.

(3) One of the following error messages.

NOT READY Disk unit is not ready and/or not on cylinder.

COMP ERR Data comparison error, An additional message is also output describing the location and actual data error. (The direction of transfer is deleted from this message)

TIME OUT	No interrupt received from controller.
INT. REJECT	Internal reject was received. 1833-4 did not respond to I/O command.
EXT. REJECT	External reject was received. 1833-4 sent a reject to an I/O command.
PROTECT S/W	Drive protect switch set during a write operation
DRIVE SEEK ERROR	Drive unit detected a seek error.
DMA ADDRESS ERROR	Attempt was made to reference non-existant memory.
DMA PARITY ERROR	Parity error occurred during read to write from main memory.
DMA PROTECT ERROR	Should never occur but indicates that an attempt was made to initiate a data transfer to protected memory with an unprotected I/O instruction.
LOST DATA	UDMA lost data condition occured.
CHECKWORD ERROR	Controller logic detected an incorrect checkword in data read from disk.
COMPARE ERROR	Indicates an error occured during a compare operation. Should never be set since test does not use the function.
DRIVE ADDRESS ERROR	Controller attempted to address a cylinder greater than last cylinder or drive.
CNTLR SEEK ERROR	Controller found after reading address field written on disk that the drive is not on expected cylinder.
INDEX/ SECTOR ERROR	An index or sector pulse was not detected.

DEVICE TRANSFER ERROR — Hardware error occurred during data transfer. No clock, dropped ready or drive fault.

REG. STATUS ERROR — One of the following registers did not agree with what was expected:

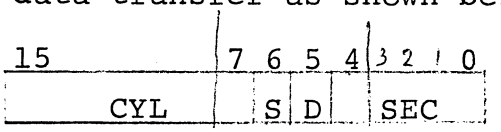
CURRENT WORD ADDRESS
CONTROLLER CYLINDER ADDRESS
CONTROLLER SECTOR ADDRESS

An additional message is output to describe the complete error (See description below).

(4) Direction of transfer

D-C Disk to core
C-D Core to disk

(5) Actual disk hardware address (hexadecimal) at the beginning of the data transfer as shown below:



Where: CYL is the drive cylinder address in the decimal range (value as hex).

1866-12 0 to 202
1866-14 0 to 405

S is the surface on the disk.

"0" = upper surface
"1" = lower surface

D is the disk.

"0" = removable
"1" = fixed

SEC is the drive sector address in the decimal range 0 to 28.

In the case of a comparison error (COMP ERR), additional messages are output in the following format:

WORD (1) WAS (2) IS (3)

where: (1) Hexadecimal number of the word with the sector where the contents were altered.

(2) Bit pattern sent to that word.

(3) Bit pattern returned fromtthat word.

When the comparison test has been completed and at least one or more comparison errors were detected, a message is output on the SLD as follows:

TSTCDD COMP ERR TOTAL (1)

where: (1) Hexadecimal total of comparison errors detected in the block being tested (range 1 - 800).

In the case of a register status error (REG. STATUS ERROR) an additional message is output on the SLD following the first error message. The format is:

(1) ADDRESS STATUS-ACTUAL (2) EXPECTED (3)

where: (1) is one of the following:

CURR WORD for a current word address register error

CNTLR CYL for a controller cylinder address register error

CNTLR SEC for a controller sector address register error

A typical error printout would be as follows:

```
TSTCDD TEST 4 RUN 0013 CHK WORD ERROR D-C XFER
    H/W ADR. 0104
TSTCDD TEST 4 RUN 0013 COMP ERR H/W ADR. 0104
WORD 0020 WAS B5A2 is B1A2
TSTCDD COMP ERR TOTAL 0001
TSTCDD TEST 4 RUN 0013 REG. STATUS ERROR D-C
    XFER H/W ADR. 0104
CURR WORD ADDRESS STATUS-ACTUAL 2F42
    EXPECTED 2F5B
```

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input six control words which specify the desired test sequence, the beginning sector address, the ending sector address, the number of times to repeat the test sequence, the controller interrupt line number and the controller WES code.

The test addresses the disk as a word addressable device (2-word address as in the 1751 Drum) instead of sector addressable (96 words/sector). Accordingly, the sector addresses are initially converted to two-word addresses which are used throughout the test. When an error is encountered, the current two-word address is converted to a hardware address (as is output to the disk controller for a load address function) plus some word number if appropraite. The resultant addresses are output in the diagnostic message.

The program jumps to each of the tests (See pages) desired by the user and outputs appropriate diagnostic messages when errors are detected. The following procedures are common to each test.

Information to be written on the disk is loaded into a fixed 2048_{10} word buffer. The variable parameters of the disk transfer callssequence are specified, and a Monitor request is executed to accomplish the transfer of the specified number of words to the specified disk area. The beginning core address for the transfer is fixed for all tests. The block of information generated for a particular test is repeatedly transferred until it has been written throughout the specified disk test area. Once this has been accomplished each block of information is regenerated and compared to that contained in the buffer. Any discrepancy between the original information and that returned from the disk results in the output of a comparison error message on the SLD.

At the completion of each transfer request, the status returned by the disk is examined for any error bits set. Any error condition results in the output of a diagnostic message that indicates the actual h/w address at which the transfer began. Any error condition will cause the transfer to be repeated once.

Upon completion of the second transfer, the program checks the disk status, outputs diagnostic messages if any errors still exist, and resumes the normal sequence. At this point, all tests conduct a comparison check. The comparison test of the original patterns and the returned patterns is conducted throughout each transferred block even though comparison

errors exist throughout the block. Comparison error messages are suppressed after the third error in a block; a tally of comparison errors for that block is computed and printed out when the comparison test is completed but only when at least one or more comparison errors were sensed in that block.

When the program completes a pass through all specified tests, it determines whether or not the test sequence should be terminated either because the test sequence has repeated the specified number of times or because the user has set thesstop flag (i.e. STOP/TSTCDD). Also, the stop flag is checked after each disk transfer.

TEST SECTION 1

Transfer 2048_{10} Word Blocks of Worst Bit Pattens

Four worst patterns are used in this test: 9555_{16}, $6AAAA_{16}$, $5A5A_{16}$, and $A5A5_{16}$. The 2048_{10} word buffer is loaded with a worst pattern and transferred to the disk until it is completely loaded. The disk is read a block at a time, and each word of the 2048_{10} word block is compared with the original pattern. This procedure is repeated for each of the four worst patterns.

TEST SECTION 2

Transfer 2048_{10} Word Blocks Containing all Ones

The 2048_{10} word buffer is filled with "1's" and transferred to the disk until it is completely loaded. The disk is read a block at a time, and each block of information is checked for all "1's".

TEST SECTION 3

Transfer 2048_{10} Word Blocks of Pseudo-Random Bit Patterns

The 2048_{10} word buffer is filled with randomly generated bit patterns and repeatedly transferred to the disk until it is completely loaded. Each block is read and compared with the original information a block at a time. A new set of random numbers is generated for each pass through this block.

TEST SECTION 4

Transfer Pseudo-Random-Length Blocks of Pseudo-Random Bit Patterns

The 2048_{10} word buffer is loaded with randomly generated bit patterns; then, successive block lengths are randomly generated, and a block is transferred for each length generated. The blocks are written on the disk so that each block begins directly following the succeeding one. When the test is completed, the random information is read a block at a time and compared with the original patterns. A new set of random patterns and random block lengths are generated for each pass through this test.

TEST SECTION 5

Transfer 2048_{10} Word Blocks Containing All Ones

The 2048_{10} word buffer is filled with "1's" and transferred to the disk until it is completely loaded. This phase is repeated ten times. The buffer is zeroed and transferred to the ds disk until it is completely loaded. The disk is read a track at a time, and each block is checked for all zeros.

TEST SECTION 6

Transfer 2048_{10} Word Blocks Containing Worst Pattern 9555_{16} to Random Addresses

The 2048_{10} word buffer is filled with the worst pattern 9555_{16}. The block is then transferred to and read from the disk at randomly generated addresses. Each block is checked for 9555_{16} throughout.

NOTES:

To convert to or from sector addressing to hardware addressing, the following should be remembered:

96 words (16 bit) per sector
29 sectors per track
2 tracks per cylinder
203 cylinders per disk (1866-12)
406 cylinders per disk (1866-14)
2 disks per drive

Normally, Disk 0 is the removable disk and disk 1 is the fixed disk.

The test routine considers the drive with two disks as one continuous medium.

There are 11774_{10} sectors on a disk therfore, the highest sector address on disk 0 is $2DFD_{16}$, the lowest sector address on disk 1 is $2DFD_{16}$ and the highest sector on disk 1 is $5BFB_{16}$.

B5F6 = Both Disks

Run time (approximate) for all disk sectors, all test sections is 3-1/2 hours.

SUPPLEMENTAL SOFTWARE

PDTCCD Physical device tables for DCYB18.
DCYB18 MSOS 5.X driver for 1833-4/1866-1X.

EXAMPLE

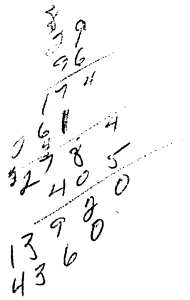
Given: 1833-4 Controller with two 1866-14 drives units 0 and 1 and one 1866-12 drive, unit 2. Controller has an equipment code of 3 and an interrupt line of 3.

```
(MI)

CONTROL WORD,PGM NAME
LOAD,TSTCCD
BEGIN 1833-4/1866-1X MULTIPLE
CARTRIDGE DISK DRIVE TEST
1833-4 INT LINE,WES CODE
3,181  (CR)
UNITS TO BE TESTED
3  (CR)
ARE PARAMETERS FOR ALL UNITS THE SAME?
YES  (CR)
PARAMETERS FOR UNIT ALL
TYPE,TESTS,BEG SEC,END SEC,RUNS
1,2,0,B7F7,1  (CR)
TSTCCD UNT 0 BEGIN
TSTCCD UNT 1 BEGIN
TSTCCD UNT 0 END,0001 RUNS,0000 ERRORS
TSTCCD UNT 1 END,0001 RUNS,0000 ERRORS
END 1833-4/1866-1X TEST
(MI)
CONTROL WORD,PGM NAME
START,TSTCCD  (CR)
BEGIN 1833-4/1866-1X MULTIPLE
CARTRIDGE DISK DRIVE TEST
1833-4 INT LINE,WES CODE
3,181  (CR)
UNITS TO BE TESTED
7  (CR)
ARE PARAMETERS FOR ALL UNITS THE SAME?
NO  (CR)
PARAMETERS FOR UNIT 0
TYPE,TESTS,BEG SEC,END SEC,RUNS
1,2,0,B7F7,4  CR
```

```
PARAMETERS FOR UNIT 1
TYPE,TESTS,BEG SEC,END SEC,RUNS
1,40,0,5BFB,100  CR
PARAMETERS FOR UNIT 2
TYPE,TESTS,BEG SEC,END SEC,RUNS
0,42,0,2DFD,1  CR
TSTCCD UNT 0 BEGIN
TSTCCD UNT 1 BEGIN
TSTCCD UNT 2 BEGIN
TSTCCD UNT 2 END,0001 RUNS,0000 ERRORS
TSTCCD UNT 0 END,0004 RUNS,0000 ERRORS
RSRCCD UNT 1 END,0100 RUNS,0000 ERRORS
```

4,521,216 WDS
PER "Drive Unit
or File"



Documentation for this test will be supplied at a later time.
Software however is currently available.

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GENERAL DESCRIPTION

The Core Resident Monitor (CRM) is a MSOS 3.0 based monitor. The following capabilities of MSOS 3.0 have been eliminated:

- Protect Processor
- System Directory
- Alternate Devices
- Core Allocation by Priority Level
- Engineering File
- Fortran Interface

The following capabilities have been added:

- Message Handler
- Dynamic Allocation of Interrupt Lines
- Dynamic Allocation of Logical Units
- Dynamic Loading of Diagnostics and Drivers
- Locore entry points for all routines used by drivers and diagnostics

The monitor performs two basic functions:

- Provides drivers for conversational devices and loader device
- Allocates the componets CRM for facilitate diagnostics routines in running a real-time environment.

The following features enable the monitor to perform these functions.

- 16 levels of program priority. System components, including input/output equipment are allocated on a priority basis.
- Highly interruptable structure; interrupts are inhibited for only short intervals.
- Monitor structure allows the computer system to be time-shared by an unrestricted number of programs.
- Re-entrant structure; monitor programs may be interrupted, called by the interrupt program, and resumed without loss of continuity.

The basic monitor structure is shown in Figure A1 and is made up in part of the following modules:

Common Interrupt Handler {Priority Structure}
Request Modules
Dispatcher
I/O Drivers

INTERRUPT LEVELS AND PRIORITIES

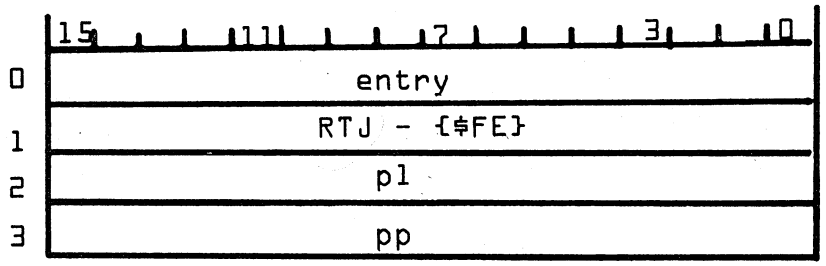
Interrupts are channeled through a central routine which saves the interrupted programs, registers and priority level in a stack. For interrupts from line zero, the internal interrupt processor is entered after stacking. The internal interrupt processor handles abnormal conditions, such as memory parity, program protect error and power failure. Memory parity and program protect errors are fatal and only cause a message to be output on TTY attempting to describe the type and probably location of the error. For interrupts from line one, the line one processor is entered after stacking. This routine determines which of the devices that can be connected to line one created the interrupt.

Interrupt lines two through fifteen are allocated by the monitor via requests from user programs. The priority and response address are passed to the allocation routine which set the trap region and the mask table.

The priority established for the interrupt lines is decided by the importance of the device or characteristics of the device. The internal interrupt of the CPU is always the highest priority interrupt (level 15). Devices that can have lost data conditions, such as unbuffered card readers and mag tape units are run at high levels (level 14). Timing devices such as System Timer are run at next lower level (13). Then comes TTY and paper tape at level (12). Other devices can use the levels 0 through 11.

COMMON INTERRUPT HANDLER

The common interrupt handler (CRMCOM) can be entered from any of the interrupt lines. Each line has a four-word interrupt trap at location 100_{16} plus line number times 4 as follows.



entry — Program address applicable at time of interrupt (the overflow bit is saved in bit 15).

#FE — FE_{16} contains address of common interrupt handler.

pl — Priority level to execute the interrupt response for this line.

pp — Address of the primary interrupt response processor. For I/O drivers this location points to a routine that is part of Physical Device Table.

The interrupt trap locations are part of the CRMSYS program. Interrupt lines 2 through 15 are initially unassigned the priority level is set to zero and the address points to involved interrupt processor INVINT. The interrupt stack is set up for all 16 interrupt lines with five words for each priority level.

When entered after an interrupt, the common interrupt handler resets overflow indicator, inhibits interrupts, and stacks the following information required to save the interrupted program.

Contents of Q register
Contents of A register
Contents of I register (memory index)
Return location and overflow indicator
Interrupt line indication (saved in memory index I after that register is saved)

The address of the next available entry in the interrupt stack is saved in location $B8_{16}$.

The new priority level is set after the required information is saved. The priority in the trap region is used as an index to the interrupt mask table (starting at location $C0_{16}$) and the M register is set to the corresponding mask. The interrupt system is then enabled and the handler exists to the primary processor address specified in Word 4 of interrupt trap with I register set to address of interrupt trap.

INTERNAL INTERRUPT PROCESSOR

The internal interrupt processor (CRMIIP) handles all internal interrupts that occur on line zero. The action taken for each type of interrupt is described below:

Memory Protect-Because the monitor is not set up to run in a protected mode, this error indicates that the protect switch is set or there was a failure in the protect system of the CPU. There is an attempt to alert the operator of the error with the following message:

PF, XXXX

Where XXXX is the contents of core location 100_{16} which is where CPU was executing when error occurred. System then hangs.

Memory Parity -This interrupt occurs when a parity error occurs in memory. There is an attempt to alert the operator of the error with the following message:

PE, XXXX

Where XXXX is the contents of core location 100_{16} which is where CPU was executing when error occurred, but may not be location of parity error because it is not the effective address for core reference instructions. System then hangs.

Power Failure -When power failure occurs, the contents of A, Q, M and I are saved along with locations zero and one. A jump to restart system is set in locations zero and one and system hangs. When power is restored and the system restarted, at location zero, manually or automatically, all registers and locations zero and one are restored and execution of monitor or user program resumes.

LINE ONE INTERRUPT PROCESSOR

The line one interrupt processor (CRMLN1) handles interrupts from input/output devices which use line one. These devices are the teletype interface and the paper tape loader.

Each device is checked to see if it has interrupt status set (if physical device table is not present, no attempt is made to check device). If the interrupt status is set, the routine schedules the driver continuator address (Word 2 of physical device table) and the driver completes the interrupt response processing.

If no device is found with an interrupt status, an invalid interrupt condition exists and control is transferred to the invalid interrupt processor which is also contained in some program.

The invalid interrupt processor alerts the operator that an unidentified interrupt occurred on an interrupt line. The routine outputs the message:

GI, X

Where X is the hexadecimal line number on which the ghost interrupt occurred. This error is not necessarily fatal, but if the condition which caused the interrupt is not reset, the message will be output continuously. If the priority level of the interrupt line is greater than that of the TTY driver, the system will hang and the message will never be output.

I/O DRIVER INTERRUPT PROCESSING

The interrupt responses for lines 2 through 15 are usually those for I/O devices that are controlled by I/O drivers. The drivers actually handle interrupt response but a small routine must reset the location of the physical device table in the Q register before jumping to the continuator address of the driver.

REQUEST MODULES

Requests are used to instruct the monitor to perform operations such as reading and writing, program scheduling, assigning and releasing allocatable core. Each type of request starts with an indirect return jump to the monitor entry for requests, location $F4_{16}$, followed by a list of parameters.

The Core Resident monitor allows for 31 request processors. Only nine are allowed in the standard monitor and requests to other than those nine will cause a request error condition to occur. This condition will cause a message to be output as follows:

RC, XXXX

Where XXXX is the address of the parameter list.

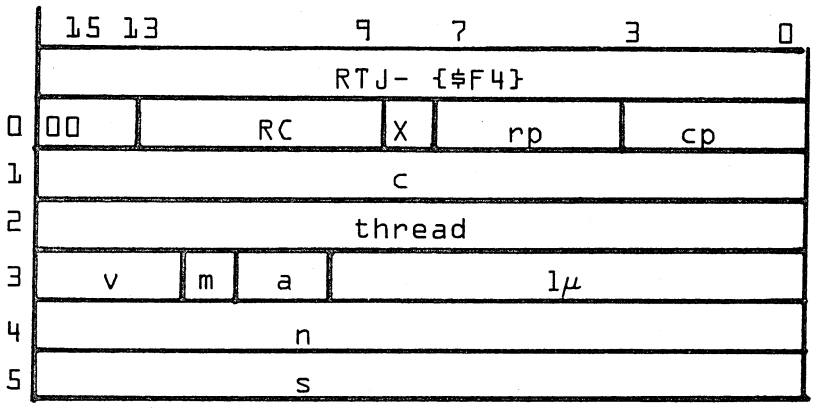
The request code is used as an index to the table of addresses of request processors. These processors are entered with the A register pointing to the parameter list, the Q register equal to the request code and the I register pointing to a volatile block of eight words requested by the monitor. Table 2.1 shows the nine standard requests allowed by CRM.

REQUEST	ENTRY POINT	DESCRIPTION
READ	T1	Read record
WRITE	T2	Write record
FREAD	T4	Read formatted record
FWRITE	T6	Write formatted record
TIMER	T8	Schedule program on a priority basis after time delay
SCHDLE	T9	Schedule program on a priority basis
SPACE	T10	Allocate core
RELEAS	T12	Release allocated core
MOTION	T14	Motion control
INDIR	None	Execute any request above {indirect}

TABLE 2.1 REQUEST DESCRIPTIONS

READ
WRITE
REQUEST
PROCESSOR

The Read-Write Request Processor {CRMRW} processes the requests for Read, Write, Fread and Fwrite. These requests all have the same basic request format.



The parameter descriptions which follow are the same for all four types of requests.

RC

1=READ
2=WRITE

These requests transfer data between the specified device and core. The word count determines the length of transfer.

4=FREAD
6=FWRITE

These requests cause records to be transferred in a specific format associated with the device specified.

rp

Request priority {0-15, 0 lowest}; priority with respect to other requests. Priority establishes position in the input/output device queue.

cp

Completion priority {0-15}; the level at which the sequence of code, specified by the parameter "C", is executed.

c

Completion address; address of core location to which control transfers when the input/output operation is complete. If C is zero, no completion routine is scheduled. {See x}

At the completion routine the "Q" register is equal to word 3 of theparameter list. The "v" field in the parameter list and in "Q" indicates the completion status.

v Completion status; bits 15-13 of word three. Meaning is as follows:

15	14	13	Description
0	0	0	No error condition detected by driver, number of words requested was transferred.
0	1	0	No error condition detected by driver, number of words transferred fewer than requested.
1	0	0	Error condition detected by driver, number of words requested were transferred, device not ready.
1	0	1	Same as above, except device was ready.
1	1	0	Error condition detected by driver, number of words transferred fewer than requested, device not ready.
1	1	1	Same as above except device was ready.

NOTE: Bits 14 and 13 have no meaning for mass memory errors.

m Mode; m=0 indicates binary mode of operation - data is transferred as it appears in the buffer; m=1 indicates ASCII mode - data in buffer is in ASCII format or data from device must be stored in buffer in ASCII format.

a Absolute/indirect indicator for the logical unit. Where a is defined as follows:

a	Description
00	1$\mu$is the logical unit
01	1$\mu$is a relative increment in the range $-1FF_{16}$ to $+1FF_{16}$ that when added to address of the first word of the parameter list will give the address of location where logical unit is stored.

10 — 1μ is an absolute address in the range 0 to $3FF_{16}$ where logical unit is stored.

11 — undefined

1μ — Logical unit number; See "a" above.

n — Number of words to transfer. {See x}

s — Starting address of data buffer. {See x}

x — Relative/indirect indicator. This parameter affects parameters "c", "s" and "n". Because of the wraparound feature, computed addresses may be before or after the parameter list.

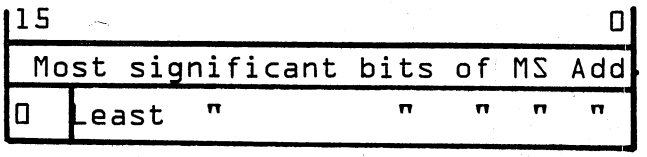
x	Definition of C
0	Completion address
1	A positive increment added to address of the first word of the parameter address list to form the completion address.

x	Definition of S
0	The starting address if bit 15=0. For mass storage, the MS address immediately follows the request, and the return is to the location following the MS address. A core address which contains the starting address if bit 15=1. For mass storage, the MS address immediately follows the location containing the starting address.
1	A positive increment added to the address of the first word of the parameter list to form the starting address, if bit 15=0. For mass storage, the MS address immediately follows the request and return is to the location following the MS address. A positive increment added to the address of the first word of the parameter list to form the address of another positive increment if bit 15=1. The second increment is added to the address of first word

of the parameter list to obtain the starting address.

For mass storage, the MS address immediately follows the location containing the second increment to the starting address.

In all cases the MS address has the following format:



The mass storage address specifies a word address on a drum or disk if the request is READ or WRITE and a sector address if a FREAD or FWRITE.

x	Definition of n
-	If bit 15=0, the length of the block to be transferred, x has no meaning.
0	If bit 15=1, a core location containing the block size.
1	If bit 15=1, a positive increment added to the address of the first word of the parameter list to obtain the address of the location containing the block size.

The Read/Write request processor queues the request on the proper logical unit thread by priority. Within a priority the requests are on a first in/first out basis. Appendix E shows an example of the queuing for RW requests.

If the driver for the logical unit is currently not busy, the initiator address of the driver is scheduled before return is made to requestor.

On return from request, the user can either continue to execute or exist to the dispatcher to wait for the request to complete.

FIND NEXT REQUEST

Drivers must dequeue requests from logical unit threads. This is done by an indirect return jump to the Find Next Request routine {CRMFNR} at $B5. This routine will dequeue the next request and fill physical device table with information from parameter list. The return is to the return address plus one. If no request is found {thread empty} the return is to the return address where normally an exist to the dispatcher is done. In both cases, on return, the I register is unchanged but A, Q and overflow are destroyed.

COMPLETE REQUEST

Drivers must complete the RW requests. This is accomplished by an indirect return jump to the Complete Request routine {CRMCRQ} at $B6. The routine puts the "v" field in the Q register and makes a secondary scheduler call by setting bit 15 of the request word {word zero of the parameter list}. The scheduler resets the bit 15 and the request is faked as a scheduler call and handled as any other scheduler request. Control is finally returned to driver. If the completion address is zero, no completion is scheduled and return is made to driver.

Find Next Request executes the following:

Resets diagnostic clock to $FFE

transfers error field in physical device table word 9, bits 15-13 to the "v" field of the request parameter list as well as Q register on completion.

Clears operation in progress flag in word 8 of physical device table.

Schedules completion address if not zero and clears thread location.

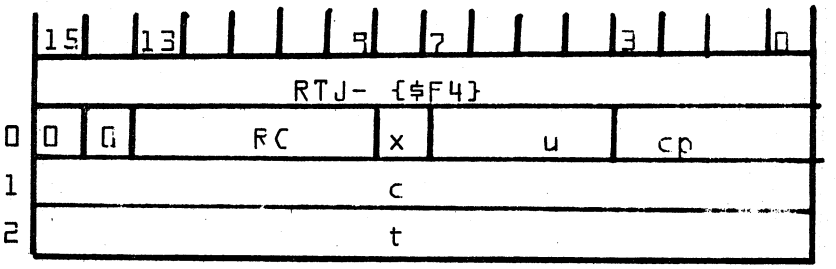
Returns to driver.

I/O ERROR HANDLING

When it is impossible to correctly complete an I/O request, most drivers will jump to the Alternate Device Handler ALTDEV and/or Engineering Log Routine LOG. These two routines will both store the error code in the LOGERR table using the logical unit as an index. If the driver goes to ALTDEV the routine completes the request in progress and schedules the driver initiater address. If the driver goes to LOG the return will be to the return address.

TIMER REQUEST PROCESSOR

The TIMER request is a delayed SCHDLE request. Through the use of TIMER, a SCHDLE request is made after a specific time delay. This request is processed by the Timer Interrupt Routine (CRMTMI). The request format is as follows:



Parameter descriptions for TIMER request are as follows:

RC = 8 request code

u — Units of delay; this parameter determines the units in which the time delay "t" is measured.

u = 0 t is basic timer units

u = 1 t is tenths of a second

u = 2 t is seconds

u = 3 t is minutes

cp — Completion priority level; this is the priority which the completion address is executed.

c — Completion address (see x)

t — Time delay

x — Relative/indirect indicator

If X=0, c is the completion address.

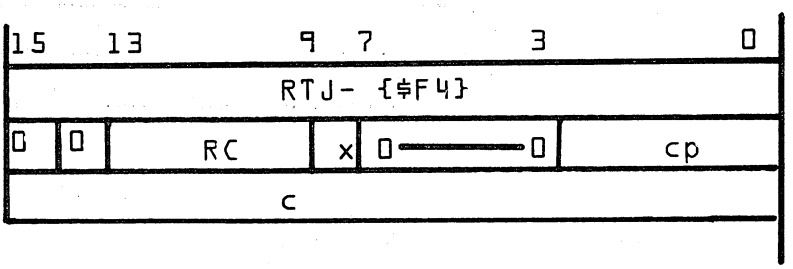
If X=1, C is a positive increment added to the address of the first word of the parameter list to obtain the completion address.

The TIMER requests are threaded by type of delays. The requests are stacked in the scheduler stack from the bottom up, on a priority basis. At

any one time, no more than five TIMER requests can be converted to SCHDLE requests. (i.e. no more than five delays can expire simultaneously).

SCHDLE REQUEST PROCESSOR

The SCHDLE request processor (CRMSCH) provides a means to queue programs on a priority basis. A program requested via SCHDLE is executed only when it is theoldest waiting task with the highest priority. The format of the SCHDLE request is as follows:



The parameter description for the SCHDLE request is as follows:

RC	=	9 request code
cp		Completion priority level; this is the priority at which the completion address is executed.
c		Completion address (See x)
x		Relative/indirect indicator If X=0, c is the completion address. If X=1, c is a positive increment added to the address of the first word of the parameter list to obtain the completion address.

The SCHDLE request processor checks each request to see if it is scheduling a program on a higher level than currently executing. If so, the current program is put on the interrupt stack and the scheduled program is executed. If the scheduled program is to be on the same or lower level, the program is queued with other waiting programs on the schedule stack. The request is moved to the stack and a return is made to the requesting program.

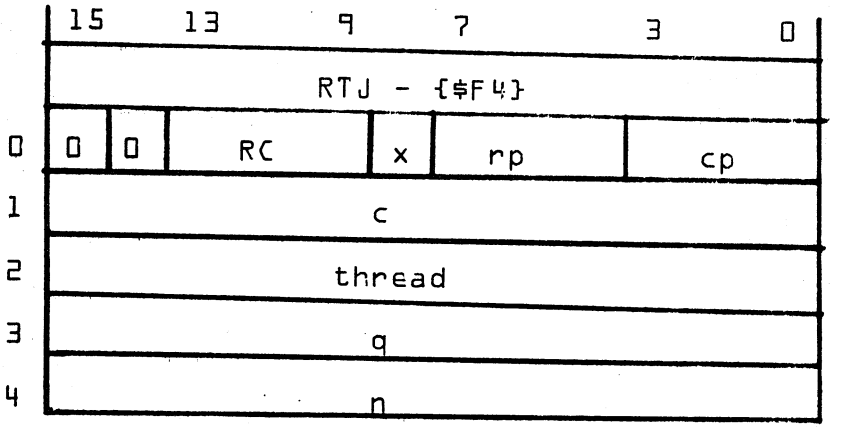
On return to the requesting program @ bit 15 is the status of the schedule request.

0 = request accepted
1 = request not accepted, no space on scheduler stack

Bits 14 to 0 are unchanged.

SPACE REQUEST PROCESSOR

The SPACE request processor allocates core on a first come, first serve basis. The SPACE request is processed by the Read/Write request processor after the return address is adjusted for a SPACE request and the logical unit is set to one. The format for a SPACE request is as follows:



The parameters for the SPACE request are defined as follows:

RC	= 10_{10} request code
rp	Request priority; priority with respect to other request. Pricrity establishes position in the core allocation queue.
cp	Completion priority; the level at which the completion address is executed.
c	Completion address {See X}

q — Address of the area allocated Set by the core driver. Also, in Q register at completion address.

If Q is positive, core was allocated.

If Q is zero, core was not allocated because there was no room currently available.

If Q is negative, core of the size requested would never be available.

n — Number of words requested.

x — Relative/indirect indicator

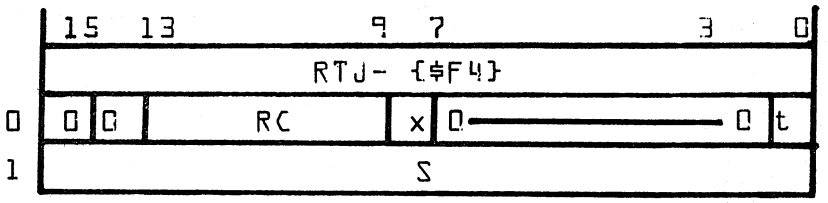
X	Definition of c
0	Completion address
1	A positive increment added to the address of the first word of the parameter list to obtain the completion address.

X	Definition of n
-	If bit 15=0, number of words of allocatable core requested, x has no meaning.
0	If bit 15=1, address of the location containing the number of words of allocatable core requested.
1	If bit 15=1, a postive increment added to the address of the first word of the parameter list to obtain the address of the location containing the number of words.

The core driver attempts to assign the smallest possible block of core to the request. It will search for an identical sized block of core or assign a block of the exact size requested.

RELEAS REQUEST PROCESSOR

The RELEAS request processor (CRMDRC) allows for the return of allocatable core when no longer needed. The format of the RELEAS is as follows:



The description of the parameters for the RELEAS requests are as follows:

RC = 12_{10} request code

t Exit indicator

0 RELEAS returns to requestor at the location following the parameter list.

1 RELEAS exits to the Dispatcher

s Starting address of the block to be released.

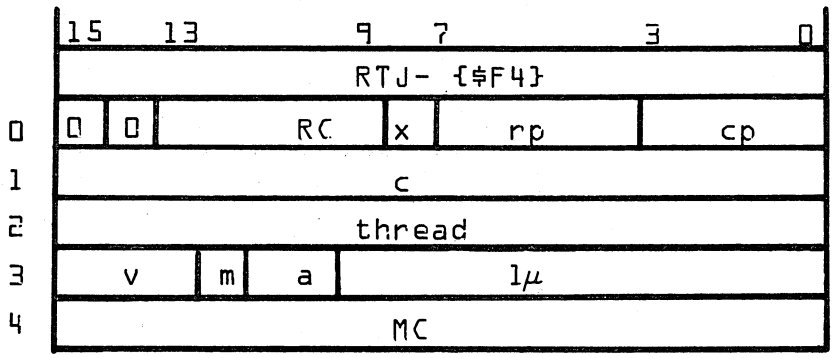
x Relative/indirect indicator

X	Definition of S
-	If bit 15=0, starting address of block to be released x has no meaning.
0	If bit 15=1, address of location containing the starting address
1	If bit 15=1, a positive increment added to the address of the first word of the parameter list to obtain the starting address.

If the starting address does not equal the start address of an allocated block of core, the RELEAS request is ignored.

MOTION REQUEST PROCESSOR

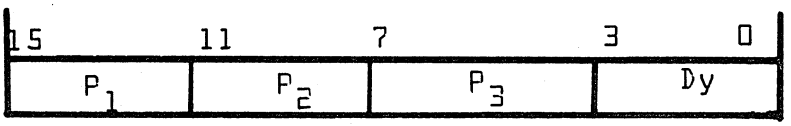
The MOTION request processor (part of CRMRW) is used to process motion control requests (especially for tape units). The format for the MOTION request is as follows:



The parameters for the MOTION request are defined identically the same as for the Read/Write/Request processor except as listed below:

RC = 14_{10} request code

MC = motion code which has two forms as shown below.



This form of the MC allows for up to three motion control commands plus a tape density section.

P_1, P_2, P_3 are three motion control codes 0-7. Normally zero indicates do nothing and/or terminate.

Dy is the density select code

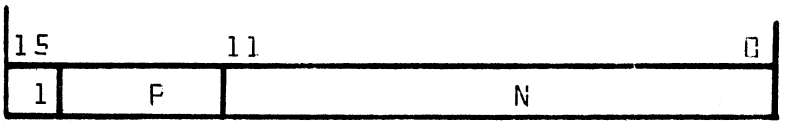
0 No change

1 800 bpi

2 556 bpi

3 200 bpi

Selecting a density not applicable to a particular tape unit may cause an external reject failure.



The form of the MC allows for repeating one MC a specified number of times.

P is same as above

N is the number of times the motion control is to be repeated.

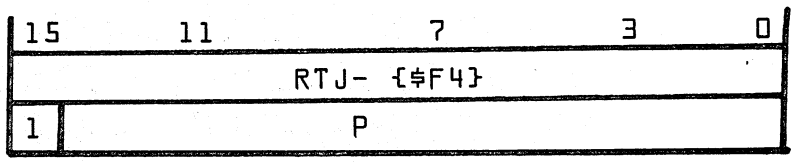
The motion control codes are defined only for tape units but are also used by other drivers for special functions. These codes are defined for tape as follows:

P	Definition
1	Backspace one record
2	Write one end-of-file mark
3	Rewind to load point
4	Rewind and unload
5	Skip one file forward
6	Skip one file backward
7	Advance one record

MOTION requests are actually processed by the Read/Write Request Processor after the return address is adjusted for MOTION request. Note: some MSOS 3.0 drivers do not check for this type of request and will execute erroneous I/O requests if MOTION requests are made to these drivers.

INDIR REQUEST

The INDIR request allows for the indirect execution of any other request as determined by the parameter list of the referenced indirect request. The format for the INDIR request is as follows:



Where p is the absolute address of the first word of the parameter list of any other request.

ISPATCHER

The DISPATCHER is entered via an indirect jump to location EA_{16}. Control transfers to the dispatcher when a program or program element terminates. The dispatcher selects the program with the highest priority from either the scheduler stack or interrupt stack. If priority in both stacks is equal, the program in the interrupt stack is selected. Control is given to the selected program at the specified priority level and address location.

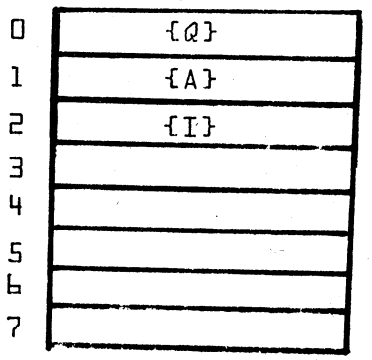
Entries are placed on the scheduler stack according to the priority of the SCHDLE request by the SCHDLE request processor. Entries are placed on the interrupt stack by the common interrupt handler or the SCHDLE request processor. When an entry is removed from either stack by the dispatcher, the next entry of the interrupt stack is at the top of the list, however, a thread determines the priority in the scheduler stack {highest priority is at the beginning of the thread.}

VOLATILE STORAGE

Volatile Storage is a storage area primarily reserved for the allocation of small blocks of data storage for routines which are reentrant {may execute at more than one priority level at same time}. Volatile storage is requested by an indirect return jump to location BB_{16}. The contents of the return address is the number of words requested. This number must be at least three. On entry, interrupts must be disabled. Sample call is shown below with example of block assigned:

```
IIN   0
RTJ-  {$BB}
NUM   8
EIN   0
```

on return I points to first word of assigned block



Volatile storage is released by an indirect return jump to location BA_{16}. On entry to release routine the I register must point to top of assigned block. On return to calling program, the registers A, Q and I are restored with values stored in Words 0, 1 and 2 of assigned volatile block. On entry to the release routine, interrupts must be disabled.

A request for more volatile storage than is available constitutes a catastrophic condition. The volatile storage assignment program enters OVFVOL with the following in the A and Q registers.

A = Amount of overflow in words
Q = Base address of volatile storage

OVFVOL {entry point in CRMOFV} clears the M register and writes OV on the comment device {the TTY}; the system then hangs.

SERVICE ROUTINES

Several special routines have been made available to program to simplify such tasks as entering parameters and outputing messages. These routines are described below:

INFOIN This routine which inputs a buffer of up to 40 ASCII characters into a buffer is entered via an indirect return jump to location 47_{16}. On entry, if the Q register equals zero, a carriage return, line feed is executed before data is input, otherwise the input is done immediately. The routine makes a formatted read request to the the input comment device.

GETFLD This routine unpacks the buffer input by the INFOIN routine and is entered via an indirect return jump to location 48_{16}. The routine unpacks hexidecimal digits from the buffer until a field delimeter is found. The last four or less digits are saved to form a hexidecimal field. On return the A register equals the field value and the Q register equals the sequential field number. The field delimeters are period, slash, comma or carriage return.

RHXASC This routine converts the value in the A register on entry to four ASCII characters stored in a two word buffer specified by the contents of the return address. The routine is entered via an indirect return jump to location 49_{16}. The routine is re-entrant and all registers are preserved on return. If the address specified in the location following the return jump is negative, the address is a relative increment from the return address to the buffer. If positive, it is an absolute address.

Sample Call:

Absolute

```
RTJ- {$49}
ADC  NAME
```

Relative

```
RTJ- {$49}
ADC  {NAME-*}
```

RODEC This routine converts the hexidecimal value in the A register to a decimal number. This routine is entered via an indirect return jump to location $4A_{16}$. The routine is re-entrant but requires a 3 word buffer for intermediate storage at the return address. The registers are not preserved. The decimal value is returned in the A register. The Q is zero on return if the number is positive or the ASCII equivalent of minus sign if the number is negative. The range of the number to be converted is ± 9999.

Sample Call:

```
RTJ- {$4A}
BZS  {3}
```

RCECHX This routine converts the decimal value in the A register to a hexidecimal number. The routine is entered via an indirect return jump to location $4B_{16}$. The routine is re-entrant and the Q and I registers are preserved. The hexidecimal number is returned in the A register. The decimal number on input has a range of 0 to 9999 only.

CLRSTK This routine clears the program name as specified in the A & Q registers and releases core for that program. This routine is entered via an indirect return jump to location $4C_{16}$. The address for core release is a sixteen bit relative address from the return address. There is no return from this routine.

Sample Call:

```
        LDA     START+1
        LDQ     START+2
        RTJ-    {$4C}
        ADC     {START-*}
```

MESAGE This routine is used to output messages. It is especially useful for messages made up of several segments. This routine is entered via an indirect return jump to location $4D_{16}$. The contents of the return address is a packed word defined as follows:

Bits 0-3	Completion Priority
Bits 4-7	Request Priority
Bits 8-11	Number of Message Segments
Bits 12-14	Not Used
Bit 15	If 1 message output on comment device if 0 message output on list device

Each message segment is specified by two words, a relative increment from the return address to the message segment followed by the length of the segment.

Sample Call:

```
        RTJ-    {$4D}
REF     NUM     $8244
        ADC     SEG1B-REF
        ADC     SEG1E-SEG1B
        ADC     SEG1B-REF
        ADC     SEG1E-SEG1B
```

The message in the above example will be output on the comment device, the combination of two segments requested a level 4 and completed at level 4. Return will be to the word following the word that specifies the length of segment 2.

Following entry to the routine, a scheduler call is executed to set level at 6. A check is then made to see if routine is busy. If not, routine continues. If busy the return address is stacked in a cylindrical table to await processing. When processing takes place, all message segments are assembled into the message buffer and one request is made to the device specified. The calling routine is then scheduled. If an error occurs during output and request was to list device, the logical unit is switched to the comment device and the request is repeated.

There are five routines provided to allow dynamic allocations of the normally fixed quantities: interrupt line, WES code, logical unit, loadable physical device tables and drivers.

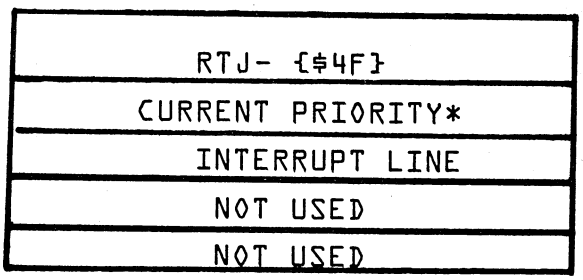
INTSEL This routine assigns interrupt lines 2 through 15 which are available for use of diagnostic routines. The routine is entered via an indirect return jump to location $4E_{16}$ followed by a four word parameter list as shown below:

RTJ- {$4E}
CURRENT PRIORITY*
INTERRUPT LINE
RESPONSE PRIORITY
RESPONSE ADDRESS

*Stored by INTSEL

The routine will set up the interrupt trap region, the Mask Table {locations $C0_{16}$ to $D0_{16}$} and the mask register {'M'register} if the interrupt line is not already assigned. If the interrupt line is assigned, a return is made to the calling program with the 'Q' register equal to $FFFF_{16}$, otherwise 'Q' equals zero on return. Return is to first word after parameter list. All registers are destroyed.

INTREL This routine releases interrupt lines assigned by INTSEL. The routine is entered via an indirect return jump to location $4F_{16}$ followed by a four word parameter list as shown below.



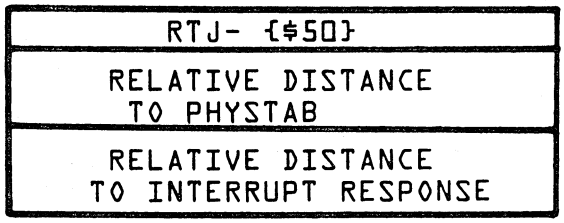
*Stored by INTREL

This routine clears Mask Table, sets the processing priority of the interrupt response to zero, sets the address of the interrupt response to the address of INVINT {ghost interrupt routine} and changes the mask register. On return, the Q register is zero and other registers are destroyed.

NOTE: When using these two routines, care should be taken not to release an interrupt line that was never assigned. INTREL does not check or have anyway of knowing if the calling routine was the one which selected the interrupt line.

DS91C

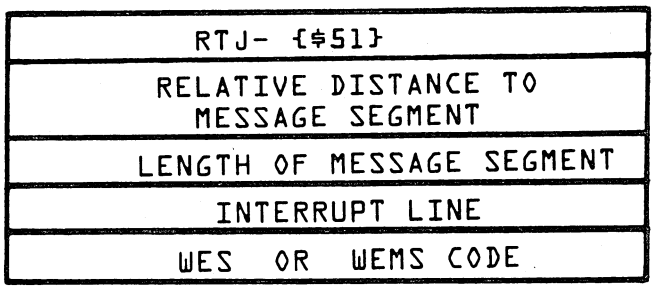
ADRABS This routine absolutizes the physical device table and interrupt response routine for a standard driver. The routine is entered via an indirect return jump to location 50_{16}. The return jump is followed by a parameter list as follows:



The routine absolutizes the parameter list, the initiator continuator and error addresses of the physical device tabs and sets the address of the PHYSTAB in the second word of the interrupt response. The two addresses following the return jump are replaced with the absolute address.

NOTE: This routine can only be entered once because all relative addresses are replaced with absolute value.

INTWES This routine outputs a request to the comment device for the input of the interrupt line and the equipment/station address for a test routine. The routine is entered via an indirect return jump to location 51_{16}. The return jump is followed by a parameter list as follows:



The routine adds message segment to message requesting parameters. If the "Q" register equals zero on entry, the message output looks as follows:

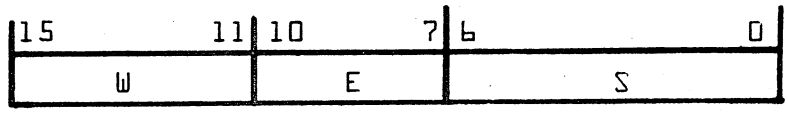
XXXXXX INT LINE, WES CODE

If the 'Q' register is non-zero on entry, the message output looks as follows:

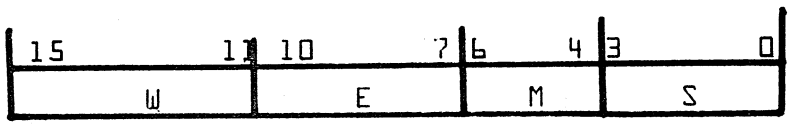
XXXXXX INT LINE, WEMS CODE

where XXXXXX indicates the message segment specified by first two words of paramter list.

The interrupt line is always entered in decimal. The line is converted to hexadecimal and checked for range of 2 through 15_{10}. A check is made if interrupt line is currently busy. The WES or WEMS code is input and stored without any checks. The WES code is that bit configuration in the 'Q' register to connect to a hardware device as:



is shown where W is the converter code (used by 1706 and 1716 only), E is the equipment code for the device and S is the station address on the device. The WEMS code is an address configuration used for the IOM (La Jolla Division built 1500 Products) hardware. This bit configuration in the 'Q' register is defined as follows:



where W is as above, E is as above except that each IOM interface (1750-1) requires two consecutive equipment codes, M is the module address M=0 for 1750-1, and S is slot address which is one of the sets of two card positions in the module specified.

On return, the 'Q' register equals zero if no interrupt error, negative zero if the interrupt line input was currently in use, negative one if the interrupt line input not in range of 2 to 15_{10}.

GETLU This routine assigns the logical units 6 to 32. This routine is entered via an indirect return jump to location 52_{16}. The routine is entered with the address of the physical device table in the 'Q' register. It assigns the first available logical unit by storing the PHYSTAB address in the corresponding location in the LOGIA and DGNTAB tables. The logical unit number is returned in the 'Q' register. If no logical unit is available, the 'Q' register is negative on return. The routine requesting the logical unit must release the logical unit by storing the address of the Dummy Driver PHYSTAB in the respective locations in the LOGIA and DGNTAB tables.

NOTE: Care should be taken not to release a logical unit not assigned.

COMMENT DEVICE DRIVER

The 1711 Teletype or the 713 CRT Display is the standard input and output comment device. The same driver handles either device. The driver will honor four requests READ, WRITE, FREAD, FWRITE. Mode has no meaning and is always assumed to be ASCII. Each request specifies the 'memory location' to read into or write from, number of words to be transferred and the completion address.

READ Request

Words in memory are filled starting at 'memory location' and continuing until the number of words specified is filled. Two characters are packed into each word. Bit

7 of each character is the parity bit and is checked for even parity before character is packed. If zero number of words is specified, one character only is read into the upper character of the specified memory location; the lower character is set to 1's.

WRITE Request

Words in memory are printed starting at 'memory location'. Each word causes two characters to be printed with the upper character being printed first. Words are printed until the number of words specified is satisfied. If zero words is specified, only the upper character of the first word is printed.

FREAD Request

Words in core are filled starting at 'core location' and continuing until the number of words specified is filled or a carriage return is encountered. Two characters are packed into each word. Bit 7 of each character is an even parity bit and is set to zero after checking it and before packing the character. If the parity bit is incorrect, a hardware error is indicated. If zero number of words is specified, one character only is read into the upper half of the specified core location. The lower character is filled with 1's. If a cancel character is encountered, character's are passed until a carriage return is detected after which the request is repeated from the beginning.* If a carriage return is not encountered before the specified numbering words have been read, characters are passed until a carriage return is encountered. The effect of the cancel character in this situation is the same as described above. Line feed characters are always ignored.

FWRITE Request

Before any characters are printed, a carriage return and line feed will be executed by the driver. The number of words is printed starting at core location specified. Each word causes two characters to be printed with the upper half being printed first. If zero number of words is specified, one character only is printed and it is the upper half of the core location specified. When a carriage return is encountered, it is executed followed by a line feed. If a character of all 1's is encountered the request is terminated.

*The caller's buffer is backgrounded with 1's prior to repeating the request.

Manual Interrupt

If a manual interrupt is detected by the comment device driver, the manual interrupt routine is scheduled.

Driver Detected Errors

Internal or External reject on input or output instructions, parity error on input, lost data and time out.

These errors are considered irrecoverable by the driver. The driver sets the error fields in the physical device table and the error parameter in the request.

Upon entry to the completion routine, the 'Q' register is negative, which indicates an irrecoverable error to user.

Status Response

The teletypewriter driver saves the latest status from the teletypewriter controller. This status is that which is returned in the A register when a status input command is executed. The driver also sets the driver detected status bits in the unused hardware bits. The status is saved in word 12 of the physical device table and is defined as follows:

STATUS BIT	CONDITION
0	Ready
1	Busy
2	Interrupt
3	Data
4	End of Operation
5	Alarm
6	Lost Data
7	Not Used
8	Not Used
9	Read Mode
10	Motor On
11	Manual Interrupt
12	No Interrupt (Set by Driver)
13	Parity Error (Set by Driver)
14	Internal Reject (Set by Driver)
15	External Reject (Set by Driver)

PAPER TAPE READER LOADER

This loader/driver controls either the 1721 or 1722 Paper Tape Reader or the reader part of the 1777 Paper Tape Station. All requests to the driver are handled as FREAD, Binary requests.

FREAD Binary Request

The first non-zero word read is interpreted as the complement of the number of words in this formatted record. This number or the number of words specified in the request parameter list, which ever is smaller, determines the number of words to be filled starting at 'core location'. Two frames fill one word with the first frame being packed into the upper half of a word. If the entire record is read, the next following word will be a checksum which will balance the sum of the header word and the information in the record to zero. If the sum is incorrect, a hardware error will be indicated. If the word count is exhausted before the end of the record, tape is passed until the end of the record if found and the checksum is checked. If the end of the record is found before the word count is exhausted, no further data is transferred and the short transfer bit is set in the 'Q' register returned at the completion address. Bit 14 is the short transfer bit. If zero number of words is specified, only one frame is read into the upper half of the specified word. The lower half is filled with 1's.

Driver Detected Errors

Internal reject on input or output instruction
External reject on input or output instruction
Alarm Condition
Lost Data
Checksum Error
Failure to Interrupt (if diagnostic timer is operational

These errors are considered irrecoverable by the driver. The driver sets the error field in the physical device table and the error parameter in the request. The Q register is set negative upon entry to the completion routine and indicates an irrecoverable error to the user.

Status response

The paper tape driver saves the latest status from the paper tape reader controller. This status is that which is returned in the A register when a status input command is executed. The driver also sets the driver detected status bits in the unused hardware bits. The status is saved in word 12 of the physical device table and is defined as follows:

STATUS BIT	CONDITION
0	Ready
1	Busy
2	Interrupt
3	Data
4	Unused
5	Alarm
6	Lost Data
7	Protected
8	Existence Code
9	Paper Motion Failure
10	Power On
11	Not Used
12	No Interrupt (Set by Driver)
13	Checksum Error (Set by Driver)
14	Internal Reject (Set by Driver)
15	External Reject (Set by Driver)

CARD READER

This loader/driver controls the 1726/405 card reader, the 1729-2 card reader, 1729-3 card reader or the reader part of the 1728/430 card reader/punch. All requests are handled as FREAD (special 8-bit format), binary requests.

FREAD Binary Request

The data read by this driver is punched in rows 2-9 on the data cards. The first two columns of the first card in the record are interpreted as the complemented number of words in this formatted record. If this word count is not negative an error is indicated. If this first word is zero, the card is passed. The data is handled as described in the paper tape reader driver. Cards are read until the end of the record is reached. These cards do not have the 7-9 binary punch indication nor do they have any kind of a sequence number. The record has a checksum as described in the paper tape driver.

Driver Detected Errors

Internal reject on input or output instruction
External reject on input or output instruction
Alarm condition
Lost Data
Checksum Error
Failure to Interrupt {if diagnostic timer is operational}

These errors are considered irrecoverable by the driver. The driver sets the error field in the physical device table and the error parameter in the request. The Q register is set negative upon entry to the completion routine and indicates an irrecoverable error to the user.

Status Response

The card reader driver saves the latest status from the card reader controller. Both level 1 and level 2 statuses are saved. These statuses are those which are returned in the A register when a level 1 or level 2 status command is executed. The driver also sets the driver detected status bits in the unused hardware bits. These statuses are saved in words 12 and 13 of the physical device table and are defined as follows.

LEVEL 1 STATUS

STATUS BIT	CONDITION
0	Ready
1	Busy
2	Interrupt
3	Data
4	End of Operation
5	Alarm
6	Lost Data
7	Protected
8	Error*
9	Motion Failure
10	End of File Switch
11	Chip Box Error {1728/430 only}
12	No Interrupt {Set by Driver}
13	Checksum Error {Set by Driver}
14	Internal Reject {Set by Driver}
15	External Reject {Set by Driver}

*When checking status, this bit can be interpreted as Pre-Read error.

LEVEL 2 STATUS
(1729-2 and 1728/430 Only)

STATUS BIT	CONDITION
0	Input Hopper Empty
1	Stacker Full
2	Fail to Feed
3	Reader Area Jam
4	Punch Area Jam (1728/430 only)
5	Stacker Area Jam
6	Pre-Read Error
7	Punch Error (1728/430 only)
8	Manual
9	Punch Inhibit Sw. (1728/430 only)
10	Interlock
11	Not Used
12	Not Used
13	Not Used
14	Not Used
15	Not Used

MAGNETIC TAPE LOADER

This loader/driver controls the 1731/601, 1732/608 or 1732-3/616-72 7-track mag tape subsystems or the 1732/609 or 1732-3/616-92/616-95 9-track mag tape subsystems. All requests that are not MOTION requests are handled as FREAD, binary requests.

FREAD Binary Request

The data read by this driver is formatted as follows: first frame, bits 15-10; second frame, bits 9-4; and third frame, bits 3-0 in upper bits of tape frame for 7 track tape and in 8-bits per frame with bits 15-8 in first frame for 9-track tape. Each data input is checked for parity. Words are input until number of words requested is satisfied or an EOP status (end of record) is received.

Driver Detected Errors

Internal reject on input or output instruction
External reject on input or output instruction
Alarm condition
Lost Data
End of File
End of Tape
Parity Error
Failure to Interrupt (if diagnostic timer is operational)

These errors are considered irrecoverable by the driver. The driver sets the error field in the physical device table and the error parameter in the request. The 'Q' register is negative upon entry to the completion routine and indicates an irrecoverable error to the user.

Status Response

The mag tape driver saves the latest status from the mag tape controller. Both level 1 and level 2 statuses are saved. These statuses are stored in a special format as shown below:

LEVEL 1 STATUS

STATUS BIT	CONDITION
0	Ready
2	Busy
3	Interrupt
4	End of Operation
5	Alarm
6	Lost Data
7	Protected
8	Parity Error
9	End of Tape
10	Load Point
11	File Mark
12	No Interrupt {Set by Driver}
13	Not Used
14	Internal Reject {Set by Driver}
15	External Reject {Set by Driver}

LEVEL 2 STATUS

STATUS BIT	CONDITION
0	556 BPI
1	800 BPI
2	Not Used
3	Seven Track
4	Write Enable
5	Not Used
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	Not Used

SYSTEM RESET ROUTINE

The System Reset Routine CRMRST is provided for resetting the system when one of the following occurs:

1. Hardware device driver hung due to lost interrupt and the diagnostic timer is not operational.

2. Constant ghost interrupt

3. Request code error

4. Protect violation

5. Parity error outside the monitor

6. Overflow of volatile storage

7. Non-monitor program executing in a non-ending loop

8. Anytime it is desired to restart the monitor

The routine resets the interrupt trap region and mask table for interrupt lines 2 through 15, resets the pointers to the interrupt stack, resets pointers and threads for scheduler stack, unthreads all I/O calls, resets the LOGIA and DGNTAB tables for logical units 6 through 32, resets core allocation thread, clears Timer threads and clears program stack area. Control is then transferred to final start-up routine in CRMSYS.

PROGRAM NAME CRMDB

MNEMONIC DB

PROGRAM FUNCTION

The Loadable Program Debug Routine CRMDB allows the operator to debug program faults on-line. The routine has several routines to facilitate this function.

Dump Core
Load Hexidecimal Numbers
Add Hexidecimal Numbers
Subtract Hexidecimal Numbers
Search Core for Number
Schedule Program

These sub-routines run at priority level 2 and may be stopped at anytime via a command from the operator.

OPERATING INSTRUCTIONS

Once CRMDB is in control, the following message is output:

START DEBUG

The operator may then type in a request which must end in a carriage return. All requests are limited to one line on the input device (72 characters max). After the request is complete and all associated messages have been output, CRMDB outputs the message

NEXT

to notify the operator that the next request may be input.

To terminate execution of CRMDB the operator inputs:

OFF (CR)

CRMDB then outputs the message:

END DEBUG

The flag word is cleared and an exit is made to the dispatcher.

If CRMDB is executing a long search or dump routine and termination is desired the operator may do as follows:

(MI)
CONTROL WORD, PGM NAME
STOP, DB (CR)

This will set the stop flag which is checked on every I/O request made from CRMDB. If the stop flag is set, CRMDB will stop as if the terminate request had been input.

If the request input was invalid (i.e. the mnemonic did not agree with one in the table) the message

DB INVALID REQUEST

is output and control is returned to NEXT.

If the request did not follow the format implicitly as shown in the request descriptions, then the message

DB FORMAT ERROR

is output and control is returned to NEXT.

If an I/O error occurs during input of a request CRMDB terminates as if the OFF request was input.

REQUEST DESCRIPTIONS

DEV, device (CR)

Allows operator to set the device to which the outputs of SCN and DPC are output. Device must equal TTY or LST, anything else will cause a format error. At load time TTY is assumed.

DPC, begin core, end core, base address (CR)

Dumps the contents of core on the device specified by the DEV request. The format is the same as OLYMPUS or UTOPIA dump routines as follows:

Address	Word 0	Word 1	Word 7
Address + 8	Word 8	Word 9	Word 15
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
Address + N-7	Word N-8	Word N-7	Word N

ADH, value 1, value 2, ... (CR)

adds a string of hexidecimal values up to 16 and outputs the answer in the format

ANS = XXXX

where XXXX is a hexidecimal number

SBH, value 1, value 2, ... (CR)

subtracts value 2 and all subsequent values up to 15 from value 1 and outputs the answer in the format

ANS = XXXX

where XXXX is a hexidecimal number.

LHX, begin core, base address/value 1, value 2, ... CR

load hexidecimal numbers into core beginning at the effective address calculated by adding base address to the beginning address. The base address need not be specified and will be set to zero. The address field and the first data field must be separated by a slash or a format error will occur. A maximum of 16 values may be entered.

SCN, begin core, end core, value, mask, increment CR

search core between limits for value specified. Only bits specified by mask are checked for equivalence. When the first equivalence is found the message

P . . . . . {P}

is output before the equivalence information. The word that is output as the contents is the unmasked word. If the increment is not specified, it is forced to one.

SCH, core address, Q reg contents, priority CR

schedules execution starting at location and priority {must be at level 3 or greater} specified, passing the Q value in the Q register.

EXAMPLES

```
MI
CONTROL WORD, PGM NAME
LOAD, DB      CR
START DEBUG
ADH, 1111, 2222, 3333     CR
ANS = 6666
NEXT
SBH, 6666, 3333, 2222, 1111   CR
ANS = 0000
NEXT
DPC, 4, 7, 21A8     CR
21AC  FFFF   FFFF    0000  0000
NEXT
SCN, 0, FFF, 0301, FF00    CR
  P    {P}
0365 0307
0789 03FB
0B2C 0342
0E57 0300
NEXT
DCP,0     CR
DB INVALID REQUEST
NEXT
OFF     CR
END DEBUG
```

PROGRAM NAME CRMLPD

MNEMONIC LPD

PROGRAM FUNCTION

The Loadable List Device Driver is a driver for the 1742-1 or 1740/501 Line Printers. The driver loads like a test routine and allows for the output of messages directed to the last device logical unit to be output on a high speed medium instead of the comment device which is normally a 10 character per second TTY.

OPERATING INSTRUCTIONS

Once the List Device Driver is in control, a request is output on the Standard Output Comment Medium (SOCM) to the user to input the hardware parameters as follows:

```
ENTER 1742 LIST DEVICE
INT LINE, WES CODE
```

The user must enter two parameters on the Standard Input Comment Medium (SICM) in the following format

(Field 1), (Field 2) CR

where Field 1 — Decimal interrupt line number is in the range of 2 to 15.

Field 2 — the WES CODE for the Director 1 Status input

CR — Carriage return

If the interrupt line is not in the range of 2 to 15 or the interrupt line is already in use, the following message is output and the parameters are requested again.

```
CRMLPD INTERRUPT ASSIGNMENT ERROR
```

If the interrupt line was legal and not in use then the address of the physical device table is set for logical unit five in both the LOG1A and DGNTAB tables. Logical unit five is set in location FB_{16}. The message

LIST DEVICE NOW 1742

is output to notify the operator that the list device is now the 1742 line printer.

If the list device driver is no longer wanted or it is desired to have all error messages on TTY, the driver may be stopped by STOP control word. The next request to the list device will cause the message

LIST DEVICE NOW TTY

to be output on the comment device to notify the user that the list device driver is now the comment device. Memory location FB_{16} is changed to logical unit four.

If the driver is restarted with the SETRUN control word, the parameters are not requested and the message informing the user of the switch in driver assignments is output.

PROGRAM DESCRIPTION

This driver can be used with both the 1740 Line Printer Controller and the 1742 Line Printer. This driver has only one mode of operation, that of non-Fortran formatted requests. That is all requests are preceeded by an upspace and all requests terminate with a print command. All I/O commands to the printer are monitored for errors. The driver develops certain error codes to describe hardware errors detected.

Driver Error Codes:

00 = Failure to interrupt (requires timer package).

02 = Alarm condition (two classes - alarm with ready and alarm without ready).

Alarm with Ready - Illegal character is transferred into memory. This alarm is cleared by Master Clear or the director functions clear controller or print.

Alarm with Not Ready - condition is paper out. Paper tear, hammer fuse or open interlock. This alarm is cleared by correction of condition followed by making the printer ready, Print director function or a Master Clear.

04 = External Reject on data transfer - attempt was made to output more than 136 characters to memory.

05 = Internal Reject - no response from printer.

06 = External Reject - function attempted on printer when printer was busy or not ready.
14 = Printer not ready.
62 = Stop flag detected.

63 = Request while list device busy from another logical unit or specified interrupt line could not be assigned.

Illegal characters - the following characters are ignored by the driver: $00-$02, $05-$0B, $0E-$1F, $7F.
Lower case characters - these characters {$60-$7E} are translated to upper case {i.e. $40-$5F}.

Control Characters - These characters are not sent to printer memory. They are used to send control functions to the printer.

Control characters are as follows:

CHAR	NAME	DESCRIPTION
$03	End of Text	Print Buffer, upspace 1 line, terminate request
$04	End of Xmsion	Same as $03
$0C	Form Feed	Format Level 1 {Top of form}
$0D	Carriage Rtn	Print Buffer, upspace 1 line.

STATUS RESPONSE

The line printer driver saves the latest status from the line printer controller. This status is that which is returned in the A register when a status input command is executed. The driver also sets the driver detected status bits in the unusual hardware bits. The status is saved in word 12 of the physical device table and is defined as follows:

STATUS BIT	CONDITION
0	Ready
1	Busy
2	Interrupt
3	Data
4	End of Operation
5	Alarm
6	Not Used
7	Protected
8	Not Used
9	6/8 Lines Coincident
10	Not Used
11	Not Used
12	No Interrupt (Set by Driver)
13	Buffer Overflow (Set by Driver)
14	Internal Reject (Set by Driver)
15	External Reject (Set by Driver)

Alarm may be caused by paper out, paper tear, fuse alarm open interlock and illegal character in buffer.

PROGRAM NAME

CRMSIC	Initializer Control Routine
CRMSRB	Relative Binary Data Processor
CRMSPT	1721/1723/1777 Paper Tape Reader/Punch Driver
CRMSCD	Card Reader/Punch Driver
CRMSMT	Mag Tape Driver
CRMSDK	Disk Driver
CRMSLP	Line Printer Driver
CRMSCT	1595/4203 Facit Cassette Output Driver
CRMSFD	Flexible Disk Driver
CRMSMG	1832-4 Mag Tape Input Driver (9 Track Only)

PROGRAM FUNCTION

CRM Initializer is loaded as described under Loading Initializer on Page D-4. It is then used to load CRRTMS routines and format them to the output device so that they may be handled by the CRRTMS loader routine. The appropriate loader routine must be included in the initializer package.

All control of the initializer is done from CRMSIC. Each entry into the beginning of this routine will cause all core below the first word of this routine to be set to zero. Therefore, this must be the first routine in the initializer. All control of the initializer is done by entering the proper control words via the TTY or the loader. If no control statements are entered paper tape is input and output and TTY is comment device.

The control statements are defined below:

* Comment statements (* must be followed by a blank). If "* blank" is entered from the TTY, loading continues under the control of the previous control statement.

* C,X,HHHH Declare list device and equipment code; X=0 - no list, X=1 - TTY, X=2 - 1742-1 line printer, X=3 - 1742-30/120, 1827-30 line printer and HHHH = WES code for list device if a line printer.

*D,HHHH Declare starting disk sector address; HHHH=first sector address. Sector address is the same as used in MSOS and OLYMPUS. Cannot be less than $13.

*I,X,HHHH Declare input device; X=1 - 1721/1777 paper tape, X=2 - 1728/430 Card reader/punch, X=3 - magnetic tape, X=4 - 1729-2, 1729-3, 1829-30/60 card readers, X=5 - 1726/405 card reader and HHHH=WES code for input device.

*L,HHHH Start or continue loading monitor - HHHH= hexadecimal core address for loading. If address is not entered (i.e. third character is a blank) current address is used.

*O,X,HHHH Declare output device; X=1 - 1723/1777 paper tape, X=2 -1728/430 card reader/punch, X=3 - 1731/601 or 1732/608/609 magnetic tape, X=4 - 1733-2/856-X cartridge disk X=5 - 1738/853/854 disk, and HHHH-WES code for output device.

*P Top of form on list device, if a 1742 printer. (This should be used in lieu of manual top of form switch when initialization is in progress.)

*R,HHHH Begin loading non-monitor loadable program block. If address is not specified (i.e. third character is a blank) $0200 is used for start address.

*S,NNNNNN,HHHH Set entry point name and address.

NNNNNN=Entry point name, HHHH=core address

*T Terminate all loading, start output mode.

*U Return to input control words from TTY.

*V Get control words from the loader.

Fields in statements are limited in number of characters entered. Hexadecimal fields are limited to four (4) entered characters. Only significant digits need to be entered, leading zeros may be omitted. Entry point name field is limited to six characters and the first character must be a letter.

All control words and program loading are checked for errors. All errors except double entry point definition and card sequence errors are reported on the TTY and control is returned to the TTY for operator action.

Error Codes are:

01	Illegal control statement
02	Unknown device type
03	WES code field error
04	Device driver not linked
05	Relocatable binary deck out of order
06	Not used
07	Illegal common or data block
08	Control statement within RBD block
09	Error in sector address field
10	Sector address less than $13
11	1728/430 Card Reader/Punch mode switch
12	Disk subsystem status error
13	Disk subsystem internal/external reject
14	Disk subsystem alarm
15	No field separator found
16	No name specified in *S statement
17	Entry point address from *S statement in error
18	Control word from loader when control at TTY
19	Sector address exceeds size of removable cartridge
20	Doubly defined entry point
21	Unpatched external references
22	Entry point table overflow
23	External reference table overflow
24	Card reader internal/external reject
25	Card reader status error
26	Loader word count error
27	Loader check sum error
28	Card reader Hollerith error
29	Card punch status error
30	Card punch internal/external reject
31	Mag tape read status error
32	Mag tape read internal/external reject
33	Mag tape end of file detected
34	Mag tape write status error
35	Mag tape write internal/external reject
36	Paper tape reader internal/external reject
37	Paper tape reader status error
38	Paper tape punch internal/external reject
39	Paper tape status error
40	Mag tape reject during rewind or write end of file

LOADING INITIALIZER

The initializer routines should be loaded into CPU memory starting at location 4000_{16} so that sufficient memory space is available for handing CRRTMS programs.

If the initializer routines have been absolutized then bootstrap routines may be used to load into core.

PAPER TAPE READER ROUTINE

This routine reads formatted binary records from the 1721 Paper Tape Reader or the reader part of the 1777 Paper Tape Station. The driver will advance frames until the first non-zero frame is encountered. This frame when combined with the following frame will be the complemented word count. This word must be negative or an error will be detected. If the word count is larger than 57, an error will be detected due to the fact that the binary record is basically a card image and therefore cannot exceed 57 words. If no error is detected in the word count, the record is read and the checksum is checked for error.

The status is monitored and checked for alarm conditions. The operator is notified if an alarm condition exists.

All data is stored within the buffer area of the initializer control routine (CRMSIC) at a location called BUFFER.

PAPER TAPE PUNCH ROUTINE

This routine punches special formatted records on the 1723 Paper Tape Punch or the punch portion of the 1777 Paper Tape Station.

If the starting address of the buffer is not zero, a header record is punched which is the first three words of the record to be punched and the length of the record to be punched.

All records will start with complemented word count and end with the complement of the checksum total. A six frame leader and a six frame trailer are punched with each record except when the starting address of the record is zero. When the starting address of the record is zero a 100 frame leader is punched.

CARD READER ROUTINE

This routine loads formatted binary cards. The word count of the binary record can not be greater than 57. (Multiple card binary records are not allowed).

If the first column does not have a 7-9 punch, it is checked for a Hollerith asterisk punch. If an asterisk is recognized, the card is read as a Hollerith card, otherwise a Hollerith error code is output.

Each time a NAM card is encountered the sequence number is set to zero. If a sequence error is encountered a message is output, but the error is not fatal.

On binary reads, the binary data is checked for correct checksum. This checksum includes the sequence/7-9 word and the word count. The word count does not include the sequence/7-9 word, the word count or the checksum.

For both modes of reading all 80 columns are read. In binary mode for records less than 57 words, the rest of the buffer area is set to zero. In Hollerith mode, Hollerith punches are converted to ASCII characters and stored two to a word. All illegal Hollerith punches are set to ASCII space.

CARD PUNCH ROUTINE

This routine punches data onto cards in a CRRTMS loadable format. If starting address is non-zero a header card in punched to identify the program

Data is punched on cards eight bits to a column using the lower eight bits on the card.

The first card starts with a complementary word count in the first two columns with the most significant bits in the first column.

The last card has checksum punched in the last two columns used. The remaining part of the last card is blank.

MAG TAPE READ ROUTINE

The magnetic tape read routine reads formatted records from the Magnetic Tape Transport. The routine inputs at a tape density of 556 BPI for seven track and 800 BPI for nine track Input is done in assembly mode.

The data is packed on tape as follows:

Word 0 = frames 0 and 1 puls bits 2-6 of frame 2
Word 1 = bits 0-1 of frame 2, plus frames 3 and 4, plus bits 5-6 of frame 5
Word 2 = bits 0-4 of frame 5, plus frames 6 and 7
This pattern is repeated, using 8 frames to form three words of data.

Before data is input, the input buffer is zeroed. A maximum of 60 words is stored in the input buffer area. The record is read to the end to verify the checksum.

The routine waits for tape motion to stop before returning to caller.

MAG TAPE WRITE ROUTINE

This writes CRRTMS loadable formats on 1731/601, 1732/608/609, 1732-3/616-72/616-9X and magnetic tape units.

On seven track units, each 16-bit word is written in 3 frames in 6, 6, 4 format, density is 556 BPI.

On nine track units, each 16-bit word is written in 2 frames in 8, 8 format, density is 800 BPI.

If the starting address is not zero, a header record of 10 words is written first. This record is made up of the first three words of the buffer. The length of the buffer is in the fourth word followed by six words of zero.

DISK DRIVER

This routine writes CRRTMS on a 1733-2/856 cartridge disk or 1738/853/854 disk. The data is written in a pseudo mag tape format.

When the starting address is zero, an autoload program is written on the first sector of the cartridge disk.

All records written on disk except autoload sector are preceded by an identification sector.

All records, except that of monitor, are also preceded by a header record containing the first three words of the actual program and the length of the record to be written.

The last program is followed by a pseudo end of file mark.

CRRTMS LOADER

The loader routine for the particular medium must be included in the relocatable binary records that are initialized.

ENTRY POINTS

Entry points for CRRTMS monitor are limited to 200_{10}.
Entry points for other programs are limited to 10_{10}.

EXTERNALS

Externals for CRRTMS monitor are limited to 400_{10}.
Externals for other programs are limited to 20_{10}.

COMMENT SHEET

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1865-1/2 FLEXIBLE DISK SUBSYSTEM TEST

PROGRAM NAME CRTFDD

MNEMONIC NAME TSTFDD

PROGRAM FUNCTION

The 1865-1/2 Test Routine is a series of tests designed to exercise and determine the performance of the 1833-5 disk drive controller and the 1865-1/2 disk drive(s). One or two flexible disks can be tested in either A/Q or DMA data transfer using the DFDD driver. The user can specify data patterns, segments of disk surface tested, word or block transfer, number of times to execute test sequences, and units to be tested.

The program exercises and monitors the performance of the following operations:

1. Core-to-disk transfers of information in 192_{10} word data blocks
2. Disk-to-core transfers of information in 192_{10} word data blocks
3. Read/Write head switching
4. AQ/Buffered and Direct Memory Access (DMA) modes of operation
5. Sector/sector, multiple sector, and multiple track modes of data transfer
6. Sequential and random sector addressing
7. Interrupt End of Operation (EOP)

Required for this test are formatted flexible disks i.e., disks with control and initialization information in CDC format pre-written on Track 0. The test allows the operator to test all 77_{10} track surfaces except Track 0.

Any errors sensed during the conduct of a test will cause appropriate diagnostics to be output on the Standard List Device (SLD). The program will diagnose any of the following discrepancies:

Load TSTFDD

1. Alteration of information during core-to-disk or disk-to-core transfers.
2. Failure of disk subsystem to respond in a reasonable time (timeout).
3. Lost data, address, seek, and data parity errors in either read or write modes.

OPERATING INSTRUCTIONS

Once TSTFDD is in control, a message is output on the Standard Output Comment Medium (SOCM) as follows:

```
BEGIN 1865-1/2 FLEXIBLE DISK DRIVE TEST
```

If the flexible disk is ready and available for use then the program will request the following control words:

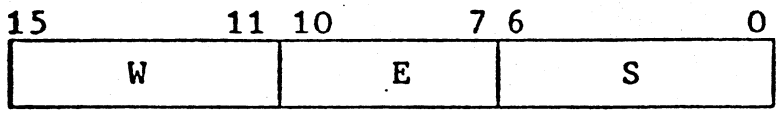
```
1865-1/2 INT LINE,WES CODE
```

The program then enables the Standard Input Comment Medium (SICM) for user keyboard input of the control words in the following format:

(Field 1),(Field 2) (CR)

where: **Field 1** The decimal interrupt line number for the 1833-5 controller; must be in the range of 2 to 15.

Field 2 1 to 4 hexadecimal digits representing the 16 bits loaded into the "Q" register to address the 1833-5 controller as shown below:



where: W = converter code which must be zero.

E = equipment number of the 1833-5 controller

S = station address - set to one by test routine

The interrupt line input is checked for correct range and if currently busy (in use). If the line number is not in range or is currently busy, the following message is output on the SOCM:

TSTFDD INTERRUPT ASSIGNMENT ERROR

The parameters are then requested again; if the error is repeated three times in succession, the test is terminated.

Following the correct input of the interrupt line number, the following message is output on the SOCM:

UNITS TO BE TESTED

Accordingly, the user must enter one control parameter on the SICM in the following format:

(Field) (CR)

Where Field is 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

Bit 0 = "1" Test Unit 0
Bit 1 = "1" Test Unit 1

The remaining bits are not used. At least one bit must be set or the parameter is requested again.

At this point a check is made to see if the system loader is a flexible disk. If it is, a warning message is output on the SOCM as follows:

BEWARE - UNIT 0 IS CRRTMS LOADER DEVICE
INPUT SCRATCH DISK AND CR WHEN READY

The user must insure that a scratch disk suitable for the test program is properly loaded in the disk drive. When the operator has met this requirement, a Carriage Return is input on the SICM.

If more than one unit was selected for testing, the following message will be output on the SOCM:

ARE PARAMETERS FOR BOTH UNITS THE SAME?

Accordingly, the user must enter one of the following via the keyboard of the SICM:

YES (CR) or NO (CR)

If YES is entered, the parameters for both units will be the same and the parameters will only be requested once. If NO is entered, the parameters will be requested for each unit to be tested.

Next, the user will be requested to input the test parameters. The following message will be output on the SOCM:

```
PARAMETERS FOR UNIT a
XFER,TESTS,BEG TRK,END TRK,RUNS
```

where a = 0 or 1 depending on the units to be tested. If YES was entered, "a" will equal both.

The SICM will then be enabled for user keyboard input of five control words in the following format:

```
(Field 1),(Field 2),(Field 3),(Field 4)
(Field 5)  (CR)
```

where: **Field 1** is one digit as follows:
Zero for A/Q data transfer where data is transferred a word at a time to the controller and a sector at a time (96 words) on the disk.
Non-zero for DMA transfer, where data is passed directly to/from the disk and memory bypassing registers in the computer and controller, allowing multisector and multi-track transfers.

Field 2 1 to 4 hexadecimal digits representing 16 bits with the following assignments:

```
Bit 1 = "1"  Do test 1
Bit 2 = "1"  Do test 2
Bit 3 = "1"  Do test 3
Bit 4 = "1"  Do test 4
Bit 5 = "1"  Do test 5
Bit 6 = "1"  Do test 6
```

The remaining bits are not assigned.

Field 3 — 2 hexadecimal digits representing the beginning disk track of the test area, may be any number between 1 and $4C_{16}$. Track 0 is reserved for control information and may not be used.

Field 4 — 2 hexadecimal digits representing the end disk track of the test area, may be any number equal to or greater than the beginning track within the range of 1 and $4C_{16}$. If the same number is used for the beginning and end track, the test area will have a dimension of one track (19_{10} sectors).

Field 5 — 1 to 4 hexadecimal digits representing number of times the test sequence is to be run. If bit 15 is set, the test will execute until halted by the user.

If the beginning disk address is larger than the ending disk address, track 0 is selected, or the address exceeds the size of the disk, the message below is output on the SOCM and the operator is requested to input the parameters again.

TSTFDD SECTOR ADDRESS ERROR

If Test 4 was selected, the following request will be output on the SOCM:

SPECIAL PATTERN FOR TEST 4

The user will then input the following on the SICM:

Field 1 (CR)

where Field 1 = 1 to 4 hexadecimal digits comprising the desired data pattern to be written on the disk.

Following acceptable input of all above test parameters, the test sequence will begin, indicated by the following message on the SOCM (one for each unit in test):

```
TSTFDD UNT a BEGIN TEST
```

where a = 0 or 1

When the test ends for a particular unit the following message is output on the SOCM:

```
TSTFDD UNT a END TEST
hhhh RUNS,hhhh ERRORS
```

where a = 0 or 1 and hhhh = some hexadecimal number

When all units have completed, the program clears the flag word and exits to the dispatcher.

ERROR MESSAGE DESCRIPTION

All error messages output by the program are output on the Standard List Device (SLD) and are of the following general format:

```
TSTFDD UNT a TEST (1)RUN(2)(3)(4) XFER
H/W ADDR (5)
```

where a is 0 or 1

(1) Decimal number of the test currently being executed

(2) Hexadecimal number of the current pass through the test sequence

(3) One of the following error messages:

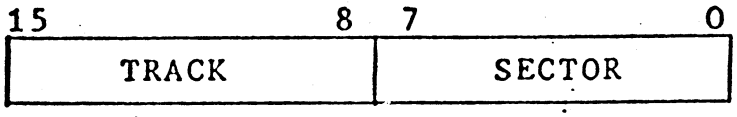
NOT READY	Disk unit not available for data transfer, can be due to improperly loaded disk, disk busy, or equipment fault.
READ/WRIT	Disk transferring data following an EOP interrupt, an illegal condition in this program.
PARITY ERR	Memory parity error detected while writing on the disk in DMA mode.
PROTECT ERR	A data transfer was initiated from unprotected core to or from a protected area.

ADDRESS ERROR	An attempt was made to reference one or more non-existant memory cells on a DMA transfer.
LOST DATA	DMA has not serviced the disk controller at the required rate.
SEEK ERROR	A track address or data record being sought cannot be found or the address returned was not expected.
CRC ERR	A CRC data read error detected on one or more data sectors.
DEL REC	Deleted record sync codes detected on disk, since none are written in this test program this would constitute a fault.
TIMEOUT	1833-5 controller did not interrupt in the expected time frame.
COMP ERR	Data comparison error. (See additional error message) The direction of transfer is deleted from this message.
INT REJ	1833-5 controller did not respond to an I/O command.
EXT REJ	1833-5 controller cannot perform the command or received an undefined command.
REG. STATUS ERROR	The current data word address did not agree with the expected value. An additional message will be output to describe error.
TRACK/SECTOR ERROR	The actual and expected disk addresses did not match following an I/O completion. Detected by driver.

(4) Direction of Transfer

D-M Disk to Memory
M-D Memory to Disk

(5) Actual disk hardware address (hexadecimal) at the beginning of the data transfer.



where:

Track is the Track address in the range of 1 to $4C_{16}$

Sector is the sector of the above track in the range of $1-13_{16}$.

In the case of a comparison error (COMP ERR) the following additional message is output on the SLD:

WORD(1) WAS(2) IS(3)

where: (1) hexadecimal number of the word within the 2 sector data block where the contents were found altered.

(2) bit pattern sent to the disk

(3) bit pattern returned from the disk

When the comparison test has been completed and at least one or more comparison errors were detected, the following message is output on the SLD:

TSTFDD COMP ERR TOTAL (1)

where (1) is the hexadecimal total of comparison errors detected in the block being tested.

In the case of a register status error, an additional message is output on the SLD following the first error message. The format is:

CURR WORD ADDRESS STATUS - ACTUAL(1) EXPECTED(2)

where (1) the actual register contents

(2) the expected register contents

A typical error printout would be as follows:

```
TSTFDD UNT 1 TEST 3 RUN 0004 PARITY D-C XFER H/W ADDR 0103
TSTFDD UNT 1 TEST 3 RUN 0005 COMP ERR H/W ADDR 0106
WORD 0020 WAS 0000 IS 0100
TSTFDD COMP ERR TOTAL 0001
TSTFDD UNT 0 TEST 4 RUN 0060 REG. STATUS ERROR
  D-C XFER H/W ADDR 0108
CURR WORD ADDRESS STATUS - ACTUAL 0102 EXPECTED 0112
```

PROGRAM DESCRIPTION

Before the test sequence can be conducted, the user must input seven control words which specify the desired test sequence, the beginning sector address, the ending sector address, the mode of data transfer, the number of times to repeat the test sequence, the controller interrupt line number and the controller WES code.

The test converts the track dimensions input by the user to sector addresses and uses these throughout the tests to address the test areas.

The program jumps to each of the tests desired by the user and outputs appropriate diagnostic messages when errors are detected. The following procedures are common to each test.

Information to be written on the disk is loaded into a fixed 192_{10} word (2 sector) buffer. The variable parameters of the disk transfer call sequence are specified, and a monitor request is executed to accomplish the data transfer to the user specified disk test area. The block of information generated is different for each test but within each test the data block is repeatedly transferred until it has been written throughout the disk test area. Once this has been accomplished, each block is read from the disk into the buffer, and the original information is regenerated and compared to that contained in the buffer. Any discrepancy between the original information and that returned from the disk results in the output of a comparison error message on the SLD.

At the completion of each transfer request, both the status returned by the disk and the status returned by the driver are examined for any error conditions detected. Any error results in the output of a diagnostic message which includes the actual h/w address at which the transfer began. Any non-recoverable type error (data, CRC, or seek error) will result in a repeated transfer attempt. Upon completion of the second transfer, the program checks the disk status, outputs diagnostic messages if any errors still exist, and resumes the normal sequence. At this point all tests conduct a comparison check. The comparison test of the original

patterns and the returned patterns is conducted throughout each transferred block even though comparison errors exist throughout the block. Comparison error messages are suppressed after the third error in a block; a tally of comparison errors for that block is computed and printed out when the comparison test is completed but only when at least one or more comparison errors were sensed in that block.

When the program completes a pass through all specified tests, it determines whether or not the test sequence should be terminated either because the test sequence has repeated the specified number of times or because the user has set the stop flag (i.e., STOP/TSTFDD). Also the stop flag is checked after each disk transfer.

TEST SECTION 1

Transfer 192_{10} Word Blocks of Worst Bit Pattern

This test loads the 192_{10} word buffer with an alternating bit pattern ($A5A5_{16}$) and transfers this data to the disk until the specified test disk area is loaded. The disk is then read a block at a time, and each word of the 192 word block is compared with the original pattern.

TEST SECTION 2

Transfer 192_{10} Word Blocks Containing All Ones

The 192_{10} word buffer is filled with "1's" and transferred to the disk until it is completely loaded. The disk is read a block at a time, and each block of information is checked for all "1's".

TEST SECTION 3

Transfer 192_{10} Word Blocks Containing All Zero's

This test is the same as test 2 except that the data patterns generated are all zero's.

TEST SECTION 4

Transfer 192_{10} Word Blocks of User-Specified Pattern

This test is the same as Test 2 except that the data pattern used in the disk-core transfers is a pattern specified by the Test Operator.

TEST SECTION 5

Transfer 192_{10} Word Blocks of Pseudo-Random Bit Patterns

The 192_{10} word buffer is filled with randomly generated bit patterns and repeatedly transferred to the disk until it is completely loaded. Each block is read and compared with the original information a block at a time. A new set of random numbers is generated for each pass through this block.

TEST SECTION 6

Transfer 192_{10} Word Blocks Containing Worst Pattern $A5A5_{16}$ to Random Addresses

The 192_{10} word buffer is filled with the worst pattern $A5A5_{16}$. The block is then transferred to and read from the disk at randomly generated addresses. Each block is checked for $A5A5_{16}$ throughout.

SUPPLEMENTAL SOFTWARE

DFDD MSOS XX driver for 1833-5/1865-X

EXAMPLE

Given: 1833-5 Controller with two 1865-X drives Units 0 and 1. Controller has an equipment code of 3 and an interrupt line of 3.

```
(MI)
CONTROL WORD,PGM NAME
LOAD,TSTFDD
BEGIN 1865-1/2 FLEXIBLE
DISK DRIVE TEST
1865-1/2 INT LINE,WES CODE
3,181    (CR)
```

```
UNITS TO BE TESTED
3    CR
ARE PARAMETERS FOR BOTH UNITS THE SAME?
YES    CR
PARAMETERS FOR UNIT ALL
XFER,TESTS,BEG TRK,END TRK, RUNS
0,2,4,7,1    CR
TSTFDD UNT 0 BEGIN
TSTFDD UNT 1 BEGIN
TSTFDD UNT 0 END, 0001 RUNS, 0000 ERRORS
TSTFDD UNT 1 END, 0001 RUNS, 0000 ERRORS
END 1865-1/2 TEST
```